

**DESIGN OF A WIRELESS VOICE  
TRANSCIVER**

**By**

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**THE UNIVERSITY OF ZAMBIA**  
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By

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**“Report submitted in partial fulfilment of requirements for the degree of  
Bachelor of Engineering, University of Zambia”.**

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To my dear mum and dad  
you have always believed in me.

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B.M

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## **LIST OF ACRONYMS**

AF	Audio Frequency
AGC	Automatic Gain Control
BPF	Bandpass filter
CDMA	Code Division Multiple Access
DC	Direct Current
DEMOD	Demodulator
DET	Detector
DPLX	Duplexer
FM	Frequency Modulation
I	In-phase
IC	Integrated circuit
IF	Intermediate frequency
IP	Third order intermodulation product
LO	Local Oscillator
LPF	Lowpass Filter
LSB	Lower Sideband
MOD	Modulator
NF	Noise Figure
PCS	Personal Communication System
Q	Quadrature
QPSK	Quadrature Phase Shift Keying
RF	Radio Frequency
RFC	Radio Frequency Choke
RX	Receiver
SNR	Signal to Noise Ratio
TX	Transmitter
UHF	Ultra High Frequency
USB	Upper Sideband
VHF	Very High Frequency

**SUMMARY**

This report details the design of a wireless voice transceiver for communication within a radius about of 20m. The transceiver has a single channel and operates in half-duplex mode. The transceiver transmits at a frequency of about 900MHz. The transceiver is built from low cost, high performance monolithic ICs that incorporate all the stages of the system.

Wireless transceivers combine transmission and reception functions allowing substantial reduction in cost and complexity along with increased ease of operation.

The design has been optimized by the use of monolithic ICs that implement the desired functions of the system to achieve these features of reduced complexity, cost and size and increased ease of operation. This is paramount for the transceiver to be operated for mobile communication.

## **CHAPTER 1 INTRODUCTION**

The transceiver is a unit in which the functions of transmission and reception are combined allowing single-channel semi-duplex operation at a substantial reduction in cost and complexity along with greatly increased ease of operation. The wireless transceiver is especially popular for mobile operation where savings in size, weight, and power consumption are important. Dual usage of components and stages in the transceiver permits a large reduction in the number of circuit elements and facilitates tuning to the common frequency desired for two-way communication.

Wireless voice transceivers are widely used by many organizations, both private and public, that depend on mobile radio systems for their successful operation. Examples are many and include (a) emergency (the ambulance, fire and police services); (b) public utilities (gas, water and electricity) ; and (c) private (delivery vans, service technicians, mini-cabs and taxis). The specifications and design of the voice transceivers will of course vary depending on the particular application.

The wireless voice transceiver design contained in this report is a half-duplex system that utilizes a single channel and operates at a frequency of 900MHz. The design has been optimised by the use of low cost, high performance ICs for most stages of the transceiver.

### **1.1 STATEMENT OF THE PROJECT PROBLEM**

The project problem statement was as follows:

Design a wireless short range voice transceiver system. The system should be able to transmit voice to other radios tuned to the same frequency. The specifications of the voice transceiver were:

- transceiver should have a single channel.
- system should use a semi-duplex mode of communication.
- design should utilize ICs where possible for circuit stages.

## 1.2 OBJECTIVES

The objectives of the project were:

- to study a communication system comprehensively
- to gain exposure to design procedures, techniques and standards
- to relate communication theory to practice.

## 1.3 SCOPE OF WORK

In order to realise the objectives of the project a number of tasks had to be performed.

A study of communication principles and techniques such as Frequency Modulation, Quadrature Modulation and the principle of operation of a superheterodyne receiver was carried out. The details are explained in Section 2.1.

The circuit of transceiver was then designed bearing the given specifications in mind.

## CHAPTER 2 LITERATURE REVIEW AND METHODOLOGY

### 2.1 LITERATURE REVIEW

A study of communication principles and techniques relevant to the design of the transceiver was undertaken. Prominent among these were Frequency Modulation, Quadrature Modulation and the Superheterodyne receiver.

#### 2.1.1 FREQUENCY MODULATION

Frequency modulation (FM) has been utilized in the transmission and reception of the baseband signal. As such it is discussed here in brief.

Frequency modulation is a form angle modulation. Angle modulated signals have the general form

$$x_c(t) = A_c \cos(\omega_c t + \Phi(t)) \quad (2.1.1.1)$$

where  $A_c$  and  $\omega_c$  are constants and the phase angle  $\Phi(t)$  is a function of the baseband signal  $x(t)$ .

The instantaneous phase of  $x_c(t)$  is defined as

$$\theta_i(t) = \omega_c t + \Phi(t) \quad (2.1.1.2)$$

and the instantaneous frequency of the modulated signal is defined as

$$\omega_i(t) = d\theta_i/dt = \omega_c + d\Phi/dt \quad (2.1.1.3)$$

The functions  $\Phi(t)$  and  $d\Phi/dt$  are referred to as the (instantaneous) phase and frequency deviations, respectively. The phase deviation of the carrier  $\Phi(t)$  is related to the baseband message  $x(t)$ . Depending on the nature of the relationship between  $\Phi(t)$  and  $x(t)$ , we have two forms of angle modulation: *phase modulation* and *frequency modulation*.

In phase modulation, the instantaneous phase deviation of the carrier is proportional to the message signal, that is,

$$\Phi(t) = k_p x(t) \quad (2.1.1.4)$$

where  $k_p$  is the phase deviation constant (expressed in radians/volt). For frequency modulated signals, the frequency deviation of the carrier is proportional to the message signal, that is

$$d\Phi/dt = k_f x(t) \quad (2.1.1.5)$$

or 
$$\Phi(t) = k_f \int x(\lambda) d\lambda + \Phi(t_0) \quad (2.1.1.6)$$

where  $k_f$  is the frequency deviation constant (expressed in (radians/sec)/volt) and  $\Phi(t_0)$  is the initial angle at  $t = t_0$ . It is usually assumed that  $t_0 = -\infty$  and  $\Phi(-\infty) = 0$ . Combining equations (2.1.1.5) and (2.1.1.6) with equation (2.1.1.1) we can express the frequency modulated signal as

$$x(t) = A_c \cos [\omega_c t + k_f \int x(\lambda) d\lambda] \quad (2.1.1.7)$$

If we assume  $x(t)$  to be sinusoidal (or a tone)

$$x(t) = A_m \cos \omega_m t \quad (2.1.1.8)$$

then the instantaneous phase deviation of the FM modulated signal is

$$\Phi(t) = (k_f A_m / \omega_m) \sin \omega_m t \quad (2.1.1.9)$$

$$x_c(t) = A_c \cos (\omega_c t + \beta \sin \omega_m t) \quad (2.1.1.10)$$

The parameter  $\beta$  is defined only for the tone modulation and it represents the maximum phase deviation produced by the modulating tone.

A tone modulated FM signal has an infinite number of sideband components and hence the FM spectrum seems to have infinite extent. Experimental evidence indicates that baseband signal distortion is negligible if 98% or more of the FM signal power is contained within the transmission band. This rule of thumb leads to useful approximate relationships between transmission bandwidth, message signal bandwidth and modulation index.

For tone modulation, the bandwidth of FM signal is given by

$$B_T \approx 2(\beta+1)f_m \quad (2.1.1.11)$$

For an arbitrary message  $x(t)$ , we can not use the preceding expression to determine  $B_T$  since  $\beta$  is defined only for tone modulation. For arbitrary message signals band limited to  $f_x$ , we can define a deviation ratio  $D$  (which is analogous to the modulation index  $\beta$ ) as

$$\begin{aligned} D &= \frac{\text{peak frequency deviation}}{\text{bandwidth of } x(t)} \\ &= \frac{k_f \max |x(t)|}{2\pi f_x} = \frac{f_\Delta}{f_x} \end{aligned} \quad (2.1.1.12)$$

Using  $D$  in the place of  $\beta$  in the equation (2.10) results in the generally accepted expression for bandwidth

$$B_T = 2(D+1)f_x \quad (2.1.1.3a)$$

$$= 2(f_\Delta + f_x) \quad (2.1.1.3b)$$

where  $f_{\Delta} = Df_x$  is the maximum frequency deviation.

FM signals are classified into two categories based on the value of  $D$  (or  $\beta$ ). If  $D$  (or  $\beta$ )  $\ll 1$ , the FM signal is called narrowband FM (NBFM) signal and the bandwidth of the NBFM is  $2f_x$ . When  $D$  (or  $\beta$ )  $\gg 1$ , the FM signal is called a wideband FM (WBFM) signal and its bandwidth is approximately  $2f_{\Delta}$ .

### 2.1.2 QUADRATURE DEMODULATION/ MODULATION

Most modern wired and wireless communication systems require sophisticated frequency conversion to and from baseband. Quadrature or I/Q modulation is frequently used by system designers to upconvert data to an intermediate frequency (IF) of anywhere from 1 MHz to several hundred MHz. Simultaneously, the receiver must downconvert the information contained at the IF and output the data in its original I/Q format. ICs that perform both these important functions are available on the market and have been utilized in this design.

#### Demodulation

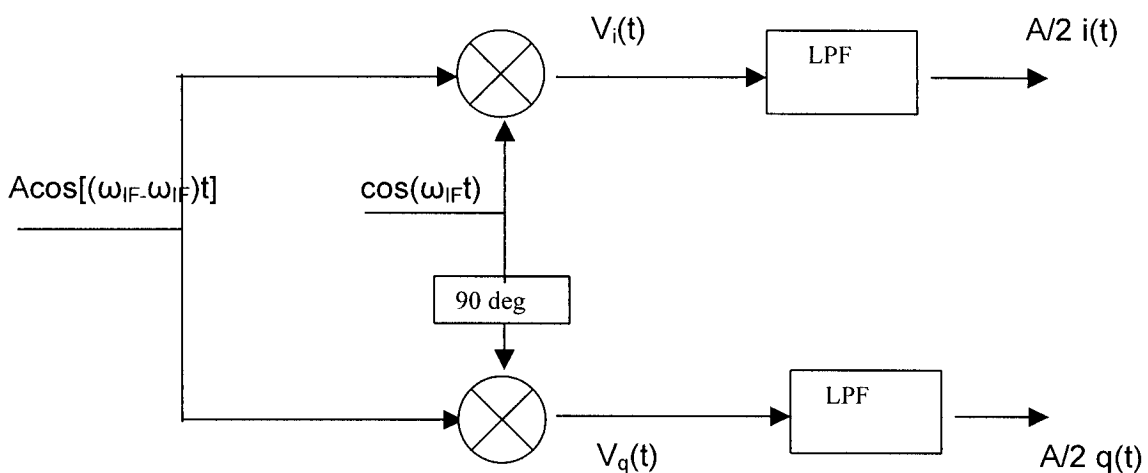


Figure 2.1.2 Quadrature demodulation operation

The following example is a simple but effective way to communicate the theory of operation of a quadrature demodulator. In the example, single sideband (SSB) modulation will be used, where the data signals,  $i(t)$  and  $q(t)$ , that are quadrature. When the IF carrier with data reaches the demodulator, it can be expressed as follows:

$$V(t) = A \cos [(\omega_{IF} + \omega_m)t] \quad (2.1.2.1)$$

where  $A$  = signal amplitude,

$\omega_{IF}$  = the IF carrier frequency, and

$\omega_m$  = the data frequency.

As shown in Figure 2.1.2, a LO signal at the IF frequency is split into an in-phase signal and a quadrature signal. These two signals are then multiplied with  $V(t)$ :

$$V_i(t) = A \cos[(\omega_{IF} + \omega_m)t] \cos(\omega_{IF}t) \quad (2.1.2.2)$$

and

$$V_q(t) = A \cos[(\omega_{IF} + \omega_m)t] \sin(\omega_{IF}t) \quad (2.1.2.3)$$

where  $V_i(t)$  = the in-phase product and

$V_q(t)$  = the quadrature product.

Using trigonometric identities:

$$V_i(t) = A/2 \cos(\omega_m t) + A/2 \cos[(2\omega_{IF} + \omega_m)t] \quad (2.1.2.4)$$

and

$$V_q(t) = A/2 \sin(\omega_m t) + A/2 \sin[(2\omega_{IF} + \omega_m)t] \quad (2.1.2.5)$$

After low-pass filtering at baseband:

$$V_i(t) = A/2 \cos(\omega_m t) = A/2 i(t) \quad (2.1.2.6)$$

$$Vq(t) = A/2 \sin(\omega_m t) = A/2 q(t) \quad (2.1.2.7)$$

Thus the demodulator has retrieved the data. The above math can be worked in reverse to illustrate SSB modulation.

### 2.1.3 SUPERHETERODYNE RECEIVERS

The receive section of the design is a superheterodyne receiver. Here the principle of operation of a superhet is given.

Besides demodulation, a typical broadcast receiver must perform three other operations: (1) carrier-frequency tuning to select the desired signal, (2) filtering to separate that signal from others received along with it, and (3) amplification to compensate for transmission loss. And at least some of amplification should be provided before demodulation to bring the signal up to the level usable by the demodulator circuitry. In theory, all of the foregoing requirements could be met with a high-gain tunable bandpass amplifier. In practice, fractional-bandwidth and stability problems make such an amplifier expensive and difficult to build. The "superhet" receiver circumvents these problems.

The superhet principle calls for two distinct amplification and filtering sections prior to demodulation, as diagrammed in Figure 2.1.3. The in-coming signal  $x_c(t)$  is first selected and amplified by a radio-frequency (RF) section tuned to the desired frequency  $f_c$ . This amplifier has a relatively broad bandwidth  $B_{RF}$  that partially passes adjacent-channel signals along with  $x_c(t)$ . Next, a frequency converter comprised of a mixer and local oscillator translates the RF output down to an intermediate-frequency (IF) band at  $f_{IF} < f_c$ . The adjustable LO frequency tracks with the RF tuning such that

$$f_{LO} = f_c + f_{IF} \quad \text{or} \quad f_{LO} = f_c - f_{IF} \quad (2.1.3.1)$$

and hence

$$|f_c - f_{LO}| = f_{IF} \quad (2.1.3.2)$$

An IF section with band  $B_{IF} \approx B_T$  now removes the adjacent-channel signals. This section is a fixed bandpass filter, called the IF strip, which provides most of gain. Finally, the IF output goes to the demodulator for message recovery and baseband amplification.

The spectral drawings in Fig.2.1.3.1 help clarify the action of a superhet receiver. Here we assume a modulated signal with symmetric sidebands and take  $f_{LO}$  so

$$f_c = f_{LO} - f_{IF}$$

The RF input spectrum in Fig. 2.1.3.1a includes our desired signal plus adjacent signals on either side and another signal at the image frequency

$$f'_c = f_c + 2f_{IF} = f_{LO} + f_{IF} \quad (2.1.3.3)$$

The main task of the RF section is to pass  $f_c \pm B_T/2$  while rejecting the image – frequency signal. For if  $f'_c$  reached the mixer, it would be down-converted to

$$f'_c - f_{LO} = (f_{LO} + f_{IF}) - f_{LO} = f_{IF}$$

and the image-frequency signal would produce an effect similar to co-channel interference. Hence, we want an RF response  $|H_{RF}(f)|$  like the dashed line, with

$$B_T < B_{RF} < 2f_{IF} \quad (2.1.3.4)$$

The filtered and down-converted spectrum at the IF input is shown in Fig. 2.1.3.1b. The indicated IF response  $|H_{RF}(f)|$  with  $B_{IF} \approx BT$  completes the task of adjacent-channel rejection.

The superheterodyne structure results in several practical benefits. First, the tuning takes place entirely in the “front end” so the rest of circuitry, including the demodulator, requires no adjustment to change  $f_c$ . Second, the separation between  $f_c$  and  $f_{IF}$  eliminates potential instability due to stray feedback from the amplified output to the receiver’s input. Third, most of the gain and selectivity is concentrated in the fixed-frequency IF strip. Since  $f_{IF}$  is an internal design parameter, it can be chosen to obtain a reasonable fractional bandwidth  $B_{IF}/f_{IF}$  for ease of implementation. Taken together, these benefits make it possible to build superhets with extremely high gain.

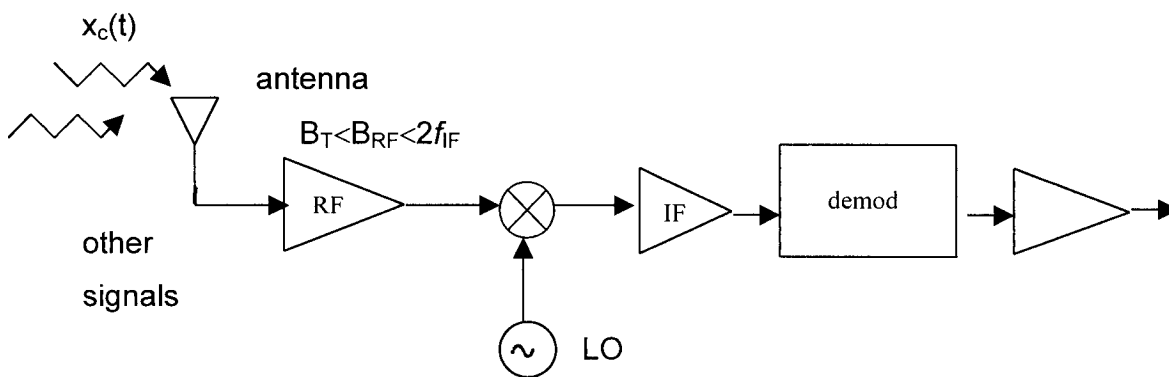


Figure 2.1.3 Superheterodyne receiver

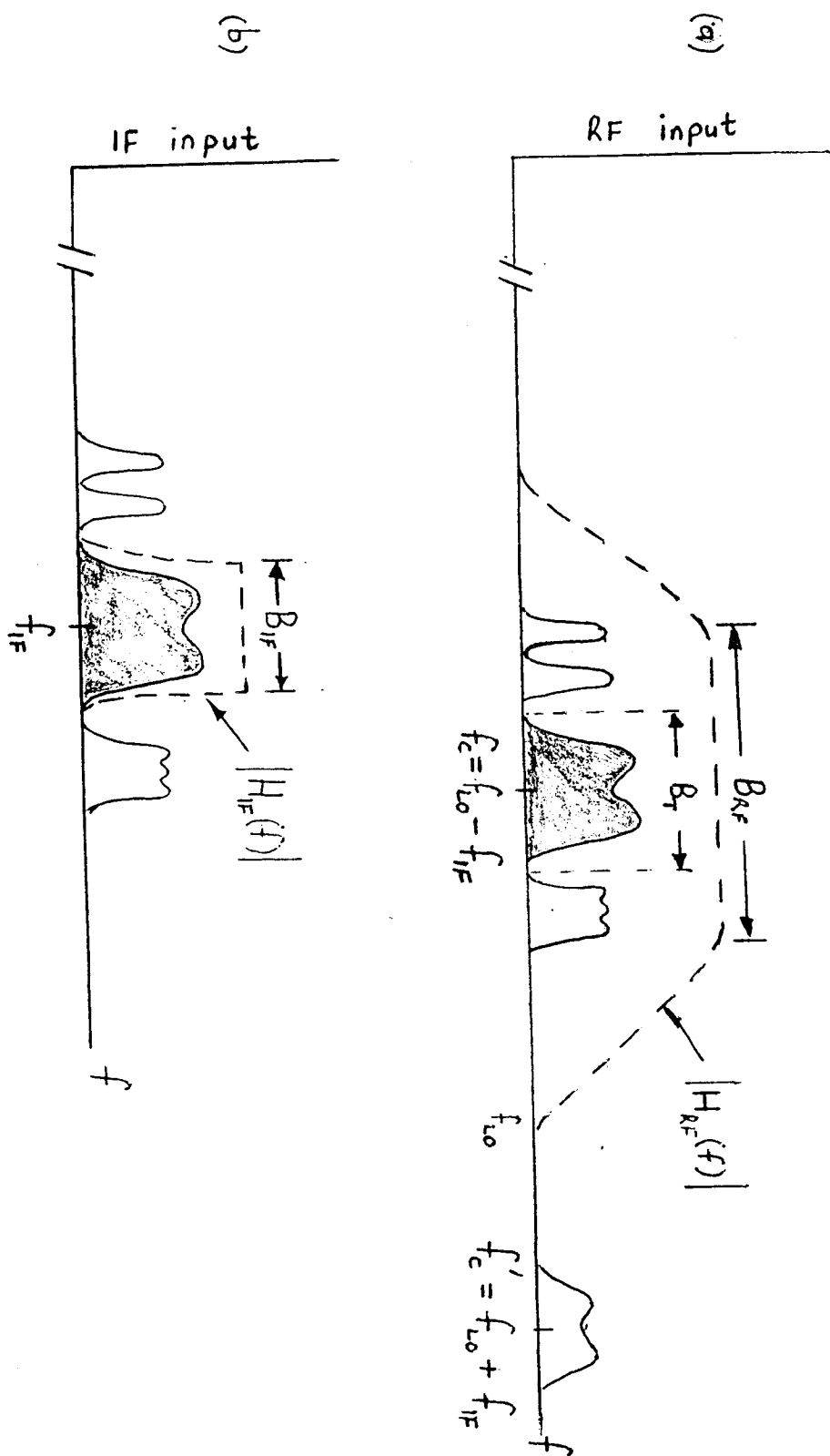


Figure 2.1.3.1

## 2.2 METHODOLOGY

Throughout the design process careful consideration was given to adhere to the given specifications of the voice transceiver. A methodology was adopted to this effect and included:

1. *Literature review:* A study of existing technology in analogue and digital transceivers and radio equipment was done. The modulation techniques were also studied and are discussed in section 2.1 of the report.
2. *Identification of appropriate ICs.* Next the appropriate ICs were selected. All the ICs selected are manufactured by RF Micro Devices<sup>®</sup>. This choice was prompted because the ICs are well matched for use in a single system and the availability of the RFMD<sup>®</sup> Designer's Handbook in time. The list of ICs used can be found in Appendix A. Appendices B-G contain the ICs data sheets.
3. *Frequency selection.* Careful selection of frequencies was undertaken. In fact this was done simultaneously as the selection of ICs was being done. Frequencies had to be chosen in such a manner that optimized the ICs selected. It was also essential to select a transmission frequency that was allowed for amateur radio operations in order to avoid procedures of getting a license from the Communication Authority. It was decided to settle for an operating frequency of 900MHz.
4. *Calculation of values for external components.* The appropriate external components (such as resistors, capacitors and inductors) to be used in conjunction with the ICs were then identified and their corresponding values calculated.
5. *Assumptions:* In recent years, the use of FM operating at 29.6MHz has become increasingly popular among amateur operators worldwide. For this reason it has been assumed that the baseband signal that is being transmitted is an FM signal of 29.6MHz. FM speech processors of this frequency are available in a number of recent Radio Handbooks.

6. *Designed System:* The circuit designed for the transceiver is given in figure 2.2.1 which shows the transmit section and figure 2.2.2 which shows the receive section. A detailed description of how the system operates is given in chapters 3 and 4.

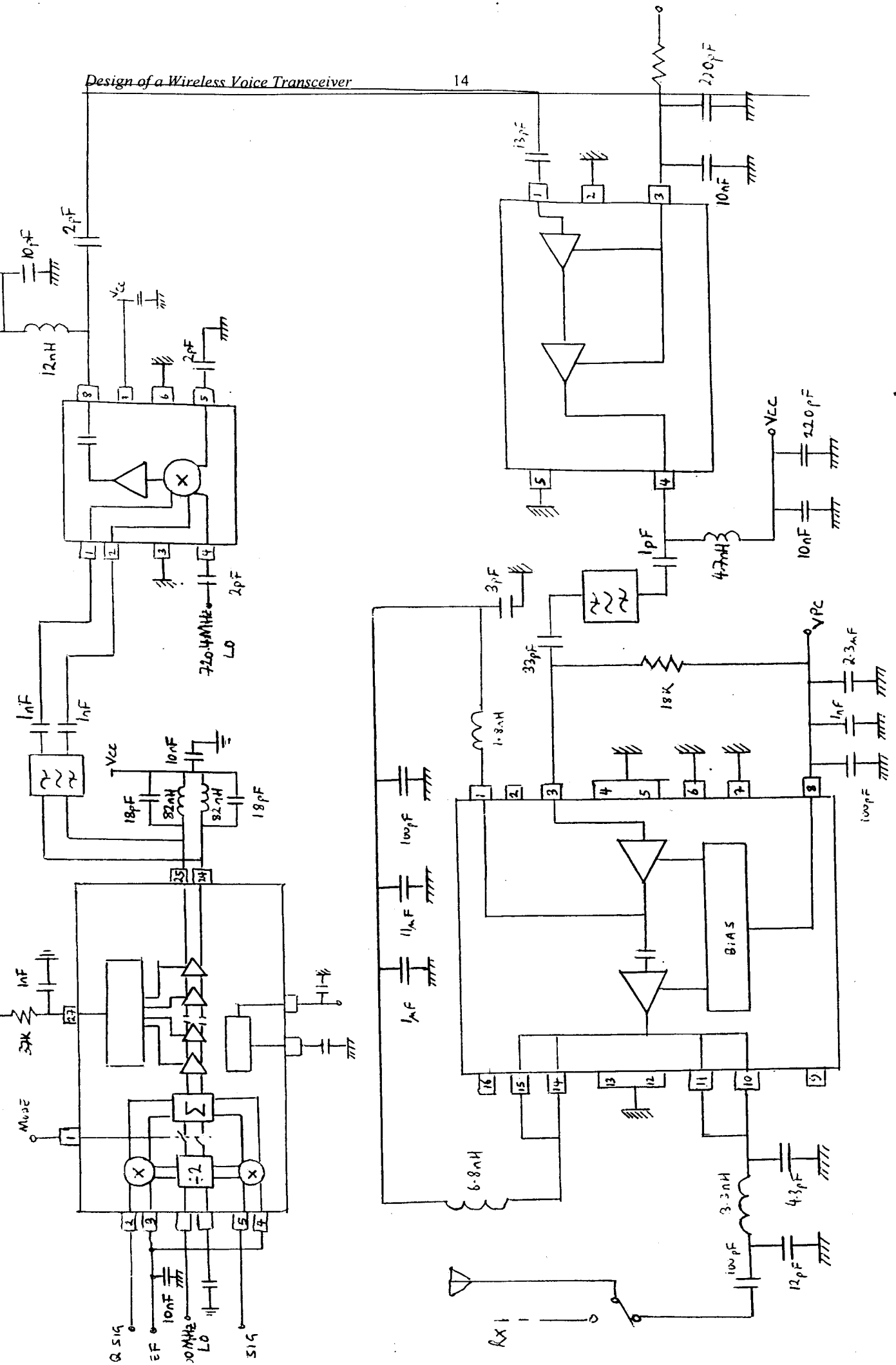


Figure 2.2.1 Transmitter Section

Design of a Wireless Voice Transceiver

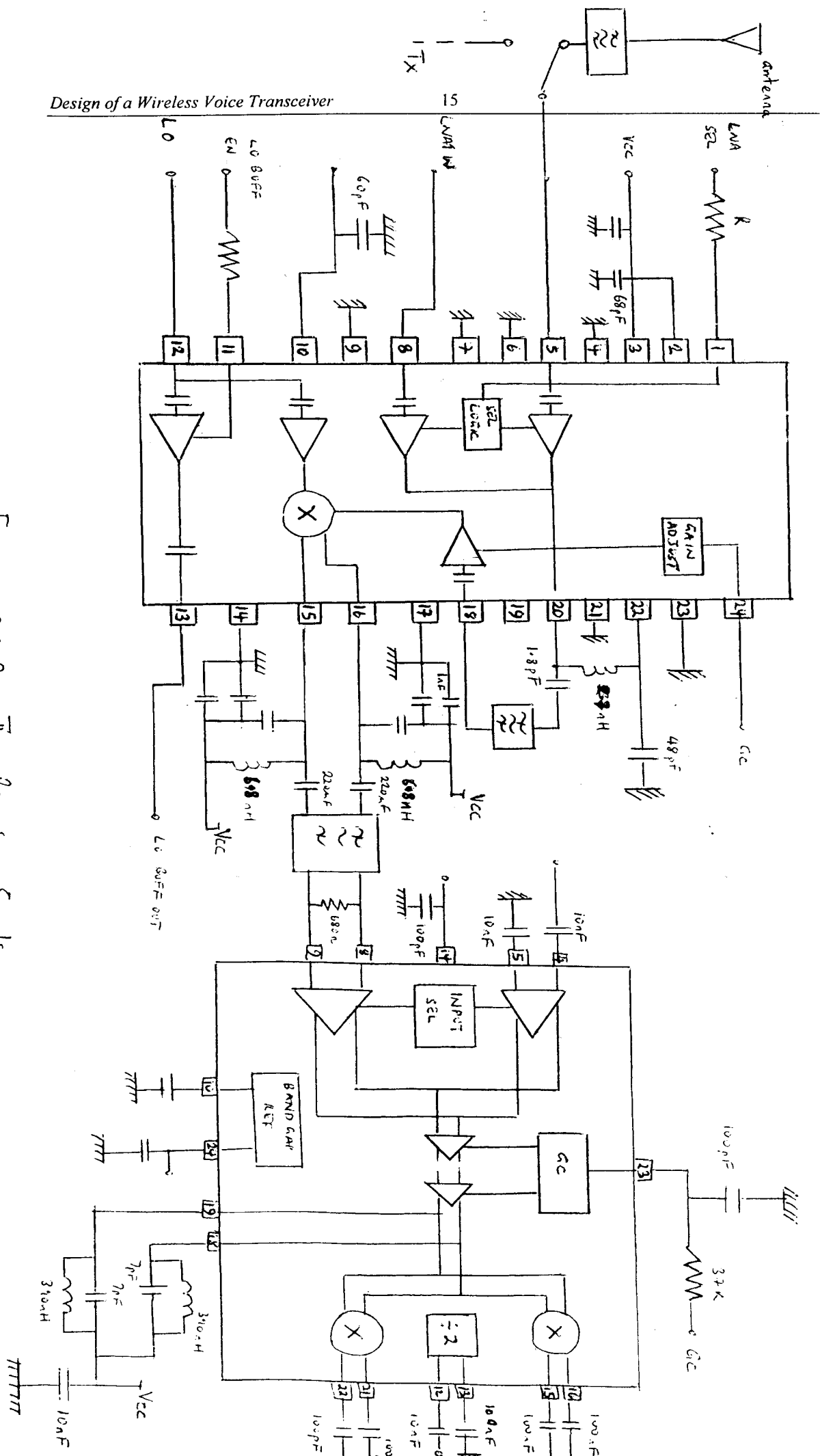


Figure 2.2.2 The Receive Section

## CHAPTER 3: THE TRANSMIT CHAIN DESIGN

The transmit chain of transceiver comprises of a transmit modulator and IF AGC IC, an upconverter, a PA driver amplifier and a PCS linear power amplifier. In this chapter these are described and their mode of operation in the design is explained.

### 3.1 TRANSMIT MODULATOR, IF AGC AND UPCONVERTOR

#### *Description*

The RF9958 was selected for transmit IC. The RF9958 is an integrated complete Quadrature modulator,IF AGC amplifier, and upconverter designed for transmit section of dual-mode CDMA/FM cellular and PCS applications. It is designed to modulate baseband I and Q signals, amplify the resulting IF signals while providing 95dB of gain control range, and perform the final upconversion to UHF. Noise figure,  $IP_3$  and other specifications are designed to be compatible with the IS-98 Interim Standards.

#### *Operation*

Figure 3.1 diagrammes the application schematic. In the transmit system the RF9958 receives baseband information of 29.6Mhz from a mixed signal in the form of in-phase/ quadri-phase (I/Q) data through pins 4 and 5. As the port is being operated single-endedly and not differentially the IREF and QREF pin are capacitively coupled to ground through C10. The I/Q waveforms are riding on a DC reference of 0.6 VDC.

The local oscillator (LO) signal onto which I/Q data is modulated is provided single-endedly through pin 8 externally and has a frequency of 300Mhz. Pin 9 (LO1-) is AC grounded by C1. The 300MHz LO signal is split into two quadrature components of 150Mhz each which are mixed with the corresponding baseband signal quadrature components to produce an IF signals of 179.6 MHz. The quadrature IF signals are then added by a balanced modulator and passed onto the gain control circuit. The capacitor C9 serves to sink AC to ground.

Pin 13 is the power down control for the overall circuit. When logic “ high” ( $\geq V_{DD} - 0.7V$ ) all circuits are operating; when logic “low” ( $\leq 0.5V$ ), all circuits are turned off. C2 and C3 are external bypass capacitors.

The IF signal output of frequency 179.6MHz is provided to the next stage of the system, which is upconversion to RF, through pins 24 and 25 through an IF filter. The IF filter filters out undesirable image channel frequencies. C4 and C5 cut out DC that is present on the IF signal.

Inductors L1 and L2 serve as RFCs that shield the IF from disturbing the VCC. For upconversion of the IF signal to RF an external upconverter is used instead of the one in-built on the RF9958 IC.

The list of values of all external components used on the RF9958 IC is found in Table A.2, Appendix A. The data sheet of the IC is in Appendix B.

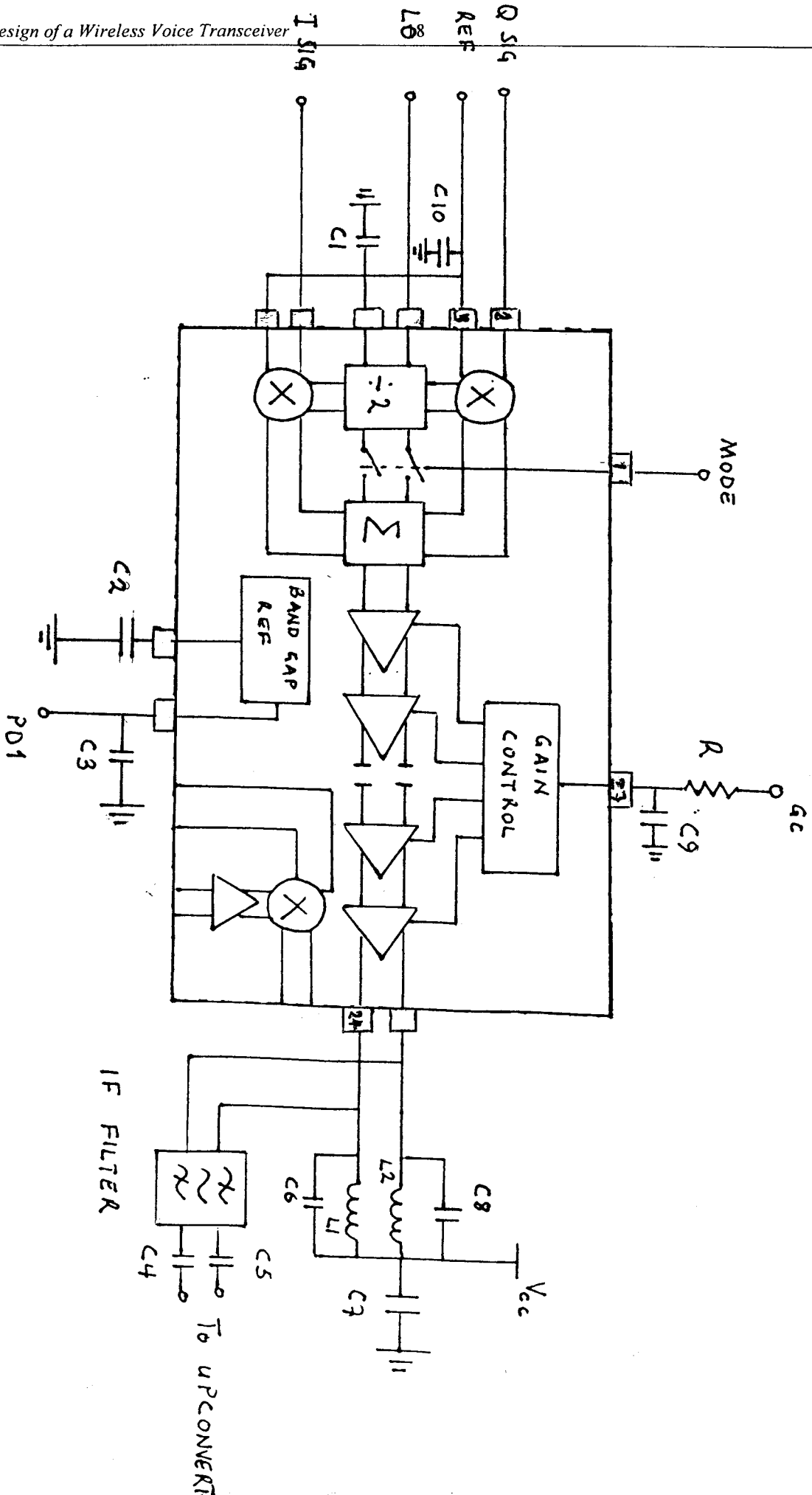


Figure 3-6 RF 9958 APPLICATION SCHEMATIC

### 3.2 THE UP CONVERTOR

#### *Description*

The RF9938 IC was selected for transmit upconversion. The RF9938 is a complete upconverter designed for PCS applications. The IC contains a double-balanced mixer stage and an output buffer amplifier stage. The mixer is a Gilbert cell with emitter degeneration resistors to provide high IP. The output stage is a class-B, push-pull configuration to reduce overall current and still provide a good 50 $\Omega$  output match.

#### *Operation*

Figure 3.2 shows the application schematic for the RF9938 Upconverter. The IF signal with frequency 179.6MHz from the transmit IC is fed to pins 1 and 2 through the capacitors C1 and C2. These pins are DC biased internally and should be DC blocked if connected to a device with a DC level present. The LO frequency is set at 720.4MHz and is sourced externally and supplied to the IC through pin 4 single-endedly as pin 5 is AC coupled to ground through C5.

The output at pin 8 is a RF signal of frequency 900MHz. The inductor L1 serves as an RFC and the capacitor C7 is DC a block.

The list that contains the description of the external components is in Table A.3, Appendix A and the data sheet of the IC is in Appendix C.

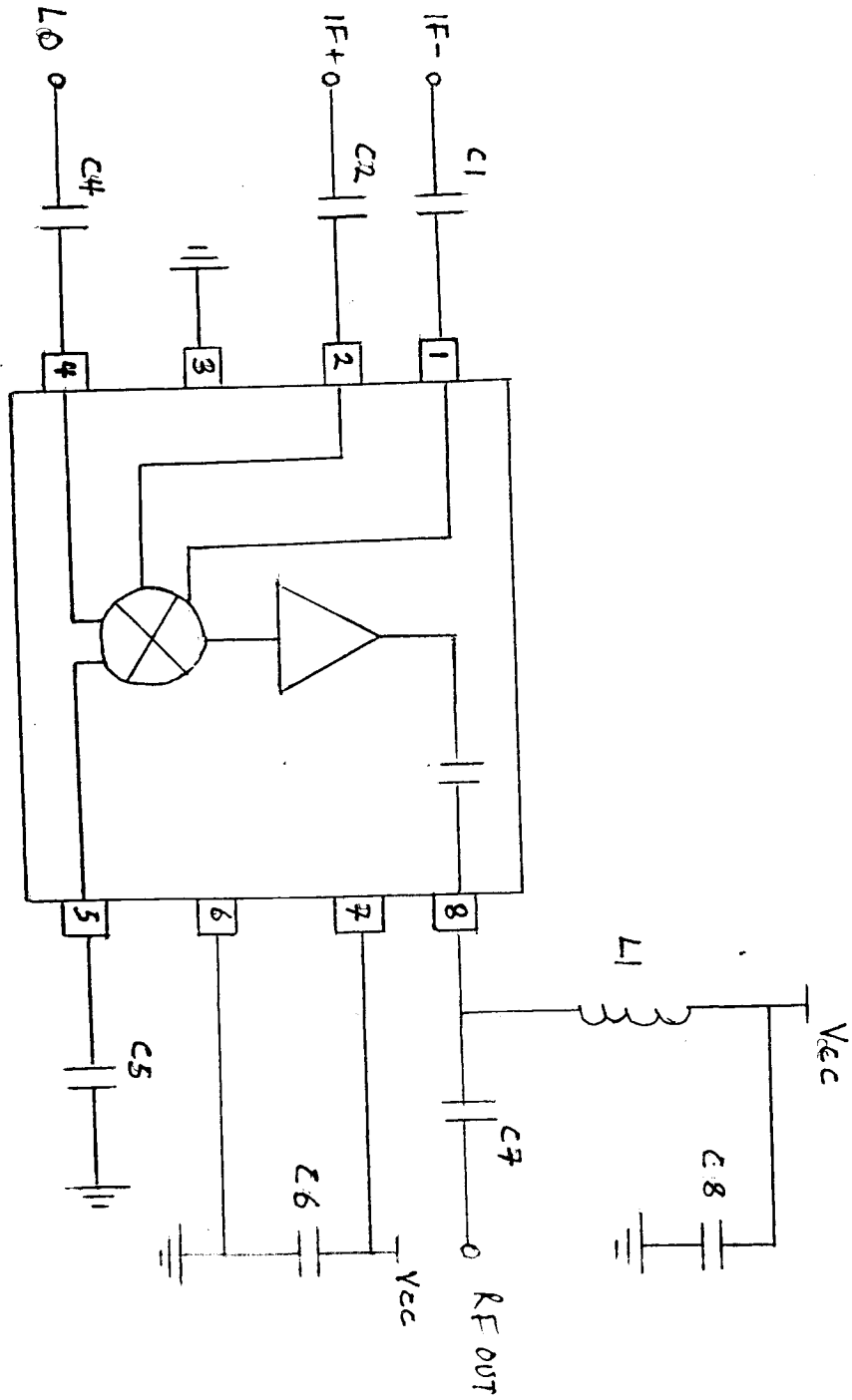


Figure 8.2 Application Schematic for RF9938

### 3.3 THE PA DRIVER AMPLIFIER

#### *Description*

The RF2362 is a low noise PA driver amplifier with a very high dynamic range for transmit PCS applications. The device functions as an outstanding PA driver amplifier in the transmit chain where low transmit noise power is a concern. The IC includes a power down feature that can be used to completely turn off the device. The IC is featured in a standard SOT23-5 plastic package.

#### *Operation*

The RF signal generated from the previous stage is driven into the RF2362 through pin 1 via a DC blocking capacitor C1. The amplifier has a typical gain of 20.3dB and a noise figure of 2.2dB for this application. The RF output is given through pin 4 and is DC blocked by C4. Pin 4 is typically matched in 50Ω with a bias matching inductor and series blocking matching capacitors C5 and C6.

Pin 3 is the power down control of the IC. The part is turned "on" when  $VPD=2.8V+0.1$ .  $VPD<0.9V$  turns "off" the part.

For the description of the external components used with the IC see Table A.4 in Appendix A. The data sheet for the IC is in Appendix D.

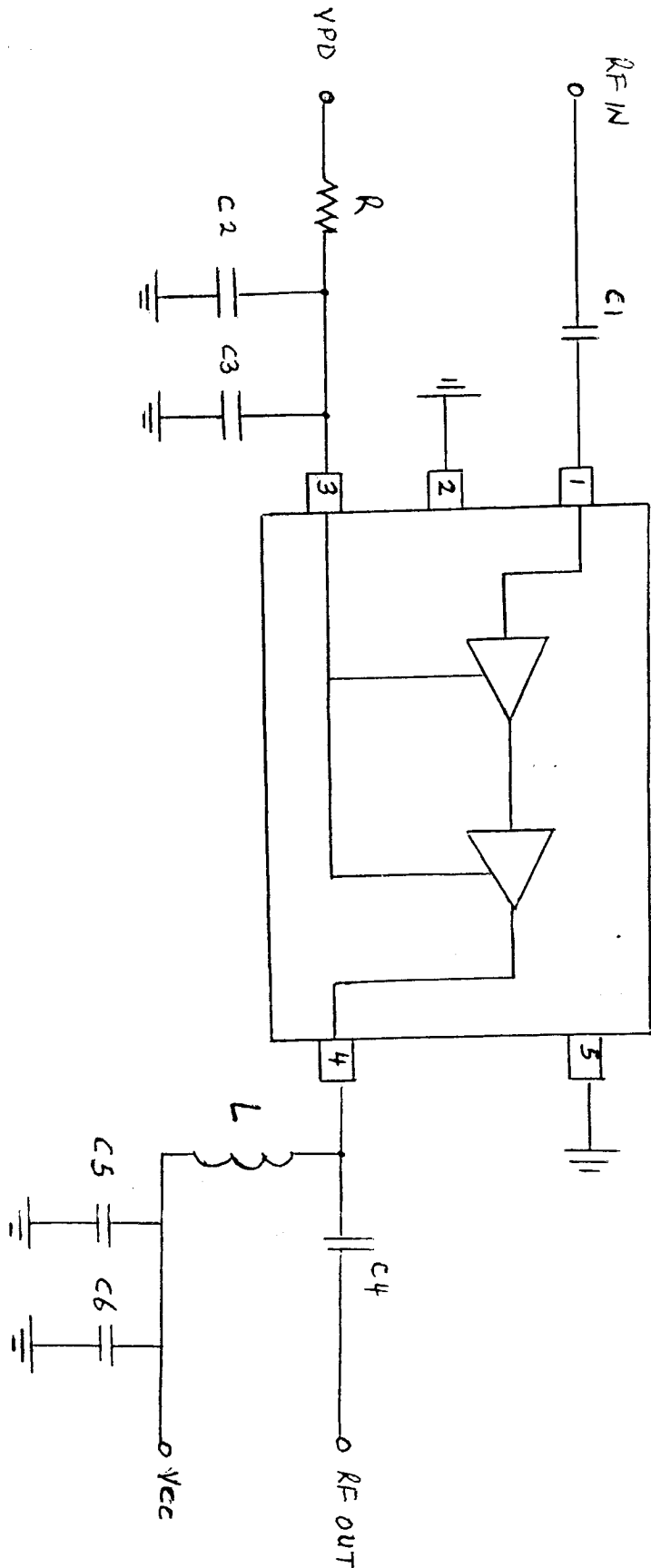


Figure 3.3 Application Schematic for RF2362

### 3.4 LINEAR POWER AMPLIFIER

#### *Description*

The RF2132 IC was chosen for the transmit power amplifier. The RF2132 is a high power, high efficiency linear amplifier IC. The device has been designed for use as the final RF amplifier in CDMA hand-held digital cellular equipment, spread spectrum systems and other applications in the 800MHz to 950MHz band. The device is self-contained with 50 $\Omega$  input and the output can be easily matched to obtain optimum power, efficiency, and linearity characteristics over varying supply and control voltages.

#### *Operation*

The filtered RF signal from RF2362 is amplified by the RF2132 before transmission to the receiver. The RF signal is supplied to the IC through pin 3. The external capacitor C8 is a DC block.

The amplified RF has its output at pin 10, which serves as power supply for the output stage. The four output pins (15, 14, 11, and 10) are combined and bias voltage for the final stage is provided through these pins. The external matching network consisting of C10, C11 and L3 provides the optimum load impedance. C9 is a DC blocking capacitor. The RF2132 provides a linear gain of about 29dB typically. L1 is a shunt inductor whilst C6 is a decoupling capacitor on the VCC side. The RF sees the decoupling capacitor as a short and is sunk to the ground whilst the DC sees it as an open circuit and is shunted to pin 1.

Table A.5 in Appendix A contains the list of description of the external components used with the IC. The data sheet of the IC is in Appendix E.

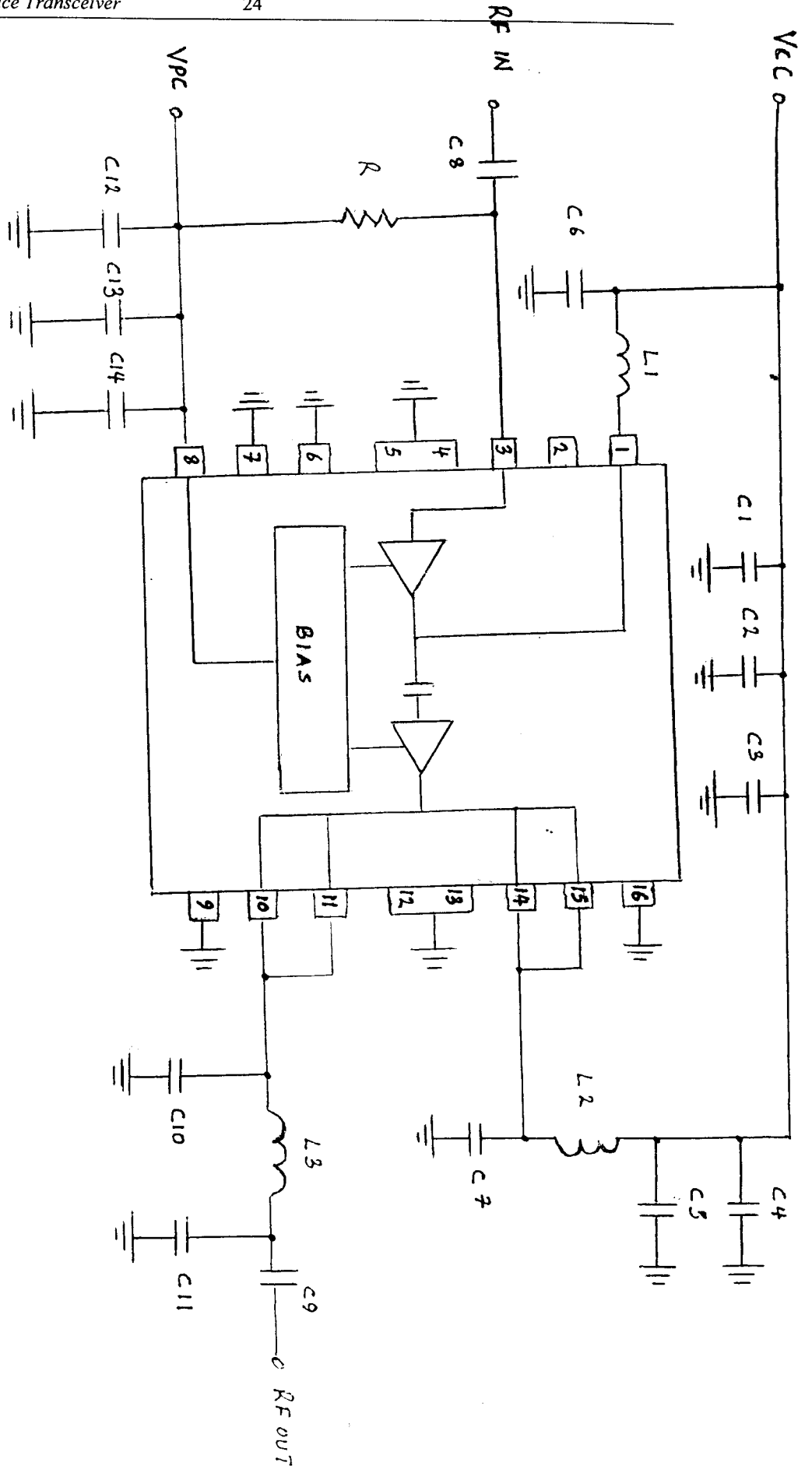


Figure 3.4 Application Schematic for RF2132

## CHAPTER 4: THE RECEIVE CHAIN DESIGN

The receive chain of the voice transceiver consists of two monolithic ICs; the PCS low noise amplifier/mixer and the Receive AGC and demodulator. In this chapter these are described and their role in the design is explained.

### 4.1 THE PCS LOW NOISE AMPLIFIER/MIXER

#### *Description*

The RF9936 was chosen for the receive chain front-end. The RF9936 is a monolithic integrated receiver frontend for PCS applications. The IC contains all of the required components to implement the RF functions of the receiver frontend except for the passive filtering and LO generation. It contains two LNAs (low noise amplifiers), a double-balanced Gilbert cell mixer, a balanced IF output, an LO isolation buffer amplifier, and an LO output buffer amplifier for providing the buffered LO signal as an output. On-chip digital logic is used to enable the appropriate LNA. The LNAs share a common output that permits insertion of a bandpass filter between the LNA output and the Mixer section. Analog gain is provided which allows a 10dB variation in gain. The IC is designed to operate from a single 3.6V power supply.

#### *Operation*

The RF signal of 900MHz is received at pin 8 and pin 5 of the IC from the antenna. Pin 1 selects which LNA to amplify the received RF signal. A logic "high" ( $>V_{CC} - 0.7V$ ) selects the upper LNA and a logic "low" ( $<0.5V_{DC}$ ) selects the lower LNA. The LNA section has a gain of 13.5dB and a noise figure of 1.4dB.

The RF output of the LNA section at pin 20 is filtered by an external SAW filter to cut out image channel and other unwanted signals. C4 serves to isolate DC from going into the filter. Filtered RF is then mixed with the LO signal to get the IF signal of  $150 + f_s$  MHz. The IF signal is filtered by an IF SAW filter before being passed on to the next stage, which is the Receive AGC and Demodulator, RF2667. The SAW

filter has considerable advantages of requiring no IF amplifier alignment and having a selectivity that is not affected by the application of AGC to the stage.

The components C5, C6, C7 and L2 and their corresponding pair C10, C11, C12 and L3 perform a filtering operation on the IF output signal. L2 and L3 in addition serve as RFCs so that the high frequency IF signal remains isolated from VCC. C5, C6, C7, C10, C11, and C12 also serve as DC blocking capacitors so that the VCC voltages are kept off ground. Figure 4.1 shows the application schematic of RF9936.

The description of the external components used with the IC is listed in Table A.6. The data sheet of the IC is contained in Appendix F.

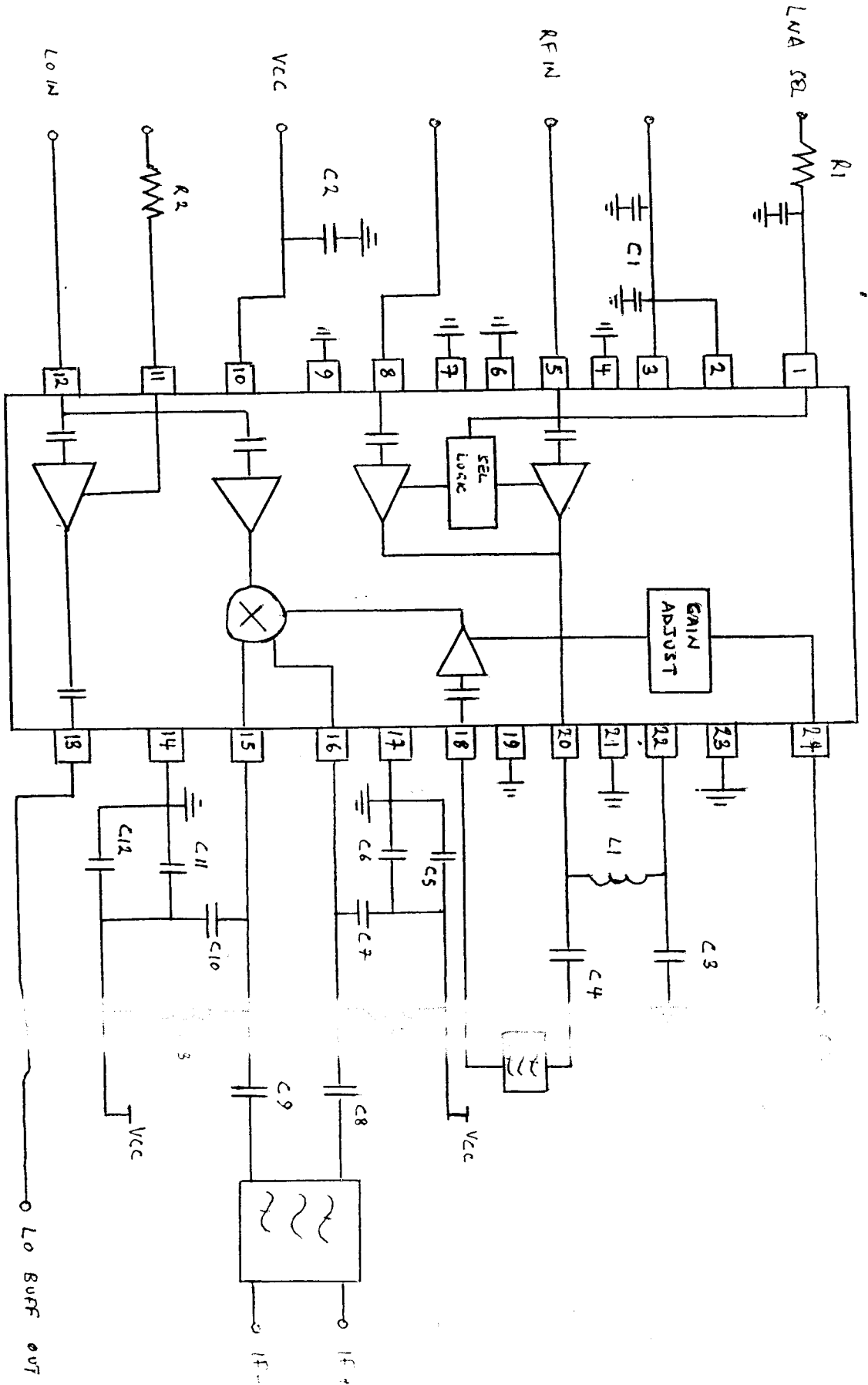


Figure 4.1 Application Schematic for RF 9936

## 4.2 THE RECEIVE AGC AND DEMODULATOR

### *Description*

The RF2667 was selected to demodulate the IF signal to baseband signal. The RF2667 is an integrated complete IF AGC amplifier and Quadrature demodulator developed for the receive section of dual-mode CDMA/FM cellular and PCS applications. It is designed to amplify received IF signals, while providing 100dB of gain control range, and demodulate to baseband I and Q signals. Noise figure, IP3 and other specifications are designed to be compatible with the IS-98 and JSTD-018 Interim Standard. The IC is packaged in a standard miniature 24-lead plastic SSOP package.

### *Operation*

The filtered IF signal of 179.6MHz from RF9936 is applied to the the IC through pins 8 and 9. Pin 14 selects CDMA mode and FM mode. A logic "high" ( $>V_{CC}-0.7V$ ) selects CDMA mode. A logic "low" ( $<0.5V_{DC}$ ) selects FM mode. FM mode is selected for this application.

The AGC is set a voltage of about 2.5VDC to get a maximum gain of 50dB. At the output of the amplifier, two pins (pins 18 and 19) are provided to allow for bandpass filtering. The parallel tank circuit comprising of L1, L2, C6 and C7 provides filtering at the receive IF frequency as well as provide a necessary DC pull-up to the power supply for the AGC output stage.

The IF signal will then enter the demodulator and mix with an LO signal. The LO signal applied at pins 12 and 13 is 300MHz which is divided into components of 150MHz and mixed with the IF signal. The output is the baseband I and Q signals at pins 21 and 22 pins 16 and 15 respectively that was transmitted.

The description of the external components used with the IC can be found in Table A.7. Appendix G contains the data sheet for the IC.

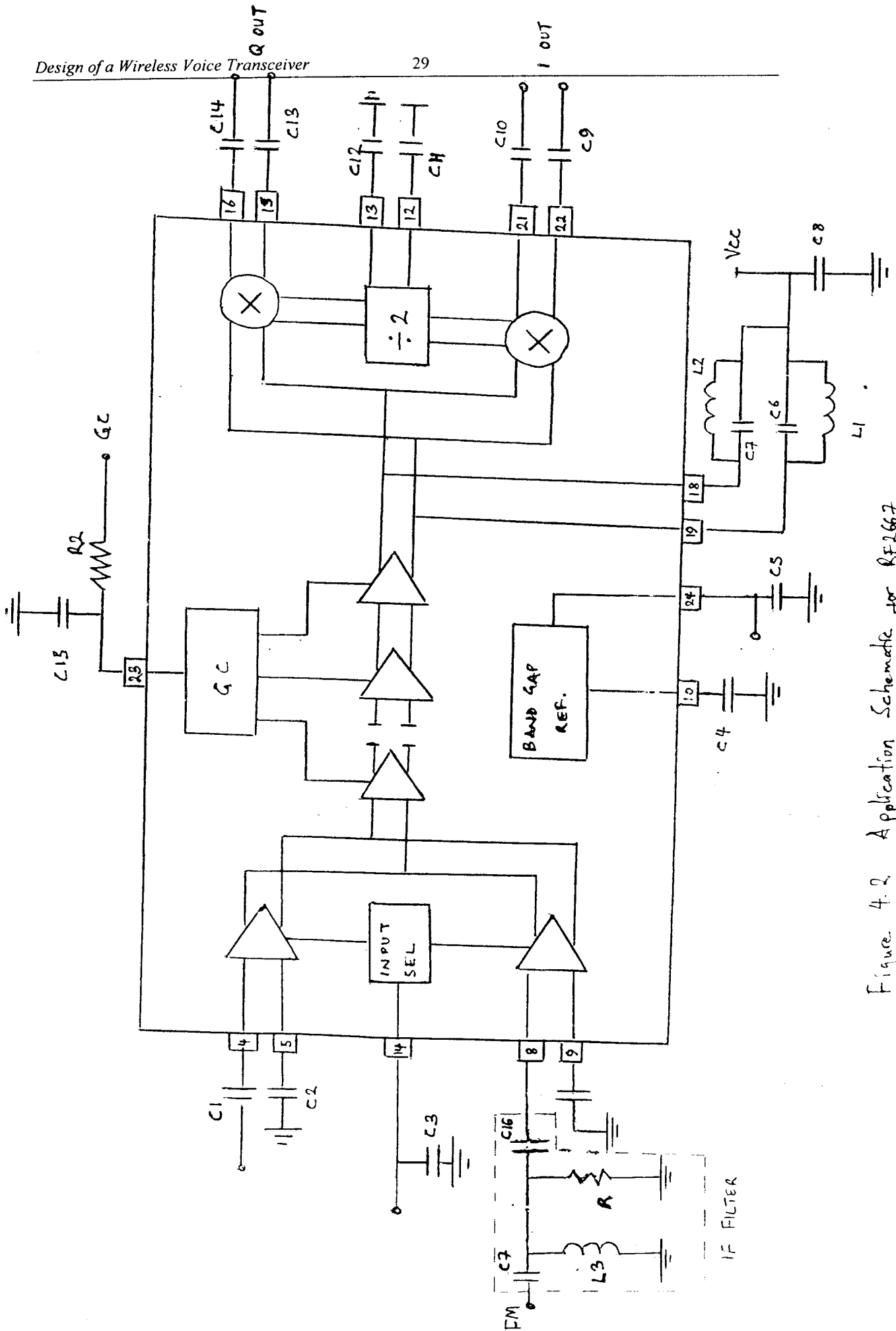


Figure 4.2 Application Schemate for RF2667

## CHAPTER 5 DISCUSSION, CONCLUSION AND RECOMMENDATIONS

### 5.1 DISCUSSION

#### *Circuitry complexity*

Every transceiver whether simple or complex, was some of the same circuitry for transmitting and receiving. Shared stages frequently include oscillators, mixers, amplifiers, filters and tuned circuits. Usually, sharing is achieved by switching the input and output of a particular stage from the receiver to the transmitter. Shared circuiting may result in more economical and compact equipment, which is ideal for a wireless device as the one designed in this report.

The designer must determine whether any transmitting and receiving stages are sufficiently alike to permit their replacement by a single circuit. To so this, three conditions must be satisfied.

First, the stages must operate in the same frequency range. Depending on the circuit, that range may be wide or narrow.

Second, input and output power levels must be comparable. Often the low level of IF signal processing that takes place in SSB transmitters allows one or more of the same IF amplifiers to be used by the receiver. However, there are other stages, such as the receiver RF amplifier and transmitter final power amplifier that are never replaced by a single circuit.

Because linearity, efficiency and heat dissipation are major concerns in SSB power amplifier design, the transistors chosen for these stages have internal geometries that optimize their power handling capability. Receiver RF amplifiers, however, process much smaller signal levels, so power handling capability is less important. Listed, great care is taken to ensure that the stage exhibits low distortion and good wire figure.

Finally, impedance must be matched. This is often done by designing each stage for an input and output impedance of  $50\Omega$ . Even when sharing is possible, it may not always be desirable. The cost complexity of the required switching circuitry and additional effort that may be needed to align the transceiving stage must be taken in account. The designer can weigh these factors against the reduction in size, weight and component cost that the transceiving approach makes possible.

#### *Justification of Assumption*

As mentioned in section 2.2 it was assumed that the baseband I and Q signals at the transmit chain input and at the receive chain output was an FM signal of about 29.6MHz. In recent years amateur radio operators have almost universally adopted 29.6MHz FM for speech signal processing in wireless communications. As such FM generation and detection circuits of this nature are readily available in recent Radio Handbooks. These circuits could be adopted for the speech processing sections of both the transmit and receive chains.

#### *Feasibility*

The design has utilized ICs for all the critical stages of the voice transceiver. Thus if at all any troubleshooting on the system it largely involve checking out the external components of the ICs. The modular approach of the design further makes troubleshooting a lot easier as it simplifies the analysis of the system. It can be easily analysed stage by stage. The use of low cost, low power, high performance ICs also provides the potential for use of the device for mobile communication.

## 5.2 CONCLUSION

The main objective of the project, which was to design a wireless voice transceiver, was attained. The system is modular and is made up of low cost, high performance monolithic ICs entirely. This is intended to develop a device that shall be used for wireless mobile communication, a phenomenon that has become very popular in this age.

## 5.3 RECOMMENDATIONS

1. The design of the transceiver does not include the transmit and receive speech processing sections. The incorporation of these two sections in the design will complete the system. They should be FM based.
2. The hardware should be built using the surface mounting technique. However for experimental purposes evaluation boards that incorporate the ICs used can be acquired at a nominal fee from RFMD™. RFMD™ can be contacted at their website [www.rfmd.com](http://www.rfmd.com).
3. Electrostatic discharge (ESD) is a major contributor to device failures. As with any integrated circuit, caution must be used when handling the RFICs. In general, the production assembly area should have static dissipative work surfaces, static dissipative floor wax, grounded work stations, and operators should utilize conductive smocks, chairs and assembly equipment.

## REFERENCES

Clarke, K.K., and D.T. Huo (1971), *Communication Circuits: Analysis and Design*, Addison-Wesley, Reading, Mass.

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RFMD, *Designer's Handbook of Wireless Components* (2000)

Shanmugam, K.S. (1979), *Digital and Analog Communication Systems*, Wiley, New York.

William, I.O., *Radio Handbook*, 23<sup>rd</sup> Ed.

## **APPENDICES**

**APPENDIX A PARTS LIST****Table A.1** List of ICs

Qty	Identity no.	Description	Manufacturer
1	RF9958	Transmit modulator, IF AGC and Upconverter	RFMD™
1	RF9938	Upconverter	RFMD™
1	RF2362	PA driver amplifier	RFMD™
1	RF2132	Linear power amplifier	RFMD™
1	RF9936	PCS low noise amplifier/mixer	RFMD™
1	RF2667	Receive AGC and demodulator	RFMD™

**Table A.2** External Components on RF9958

Part no.	Value	Part no.	Value	Part no.	Value
C1	1nF	C6	18pF	L1	82nH
C2	10nF	C7	10nF	L2	82nH
C3	1nF	C8	18nF	R	10K,27K
C4	2.2nF	C9	10nF		
C5	2.2nF	C10	1nF		

**Table A.3** External Components on RF9938

Part no.	Value	Part no.	Value	Part no.	Value
C1	1nF	C6	10nF	L1	12nH
C2	1nF	C7	2pF	R	
C4	2pF	C8	10nF		
C5	2pF				

**Table A.4** External Components on RF2362

Part no.	Value	Part no.	Value
C1	13pF	C5	220pF
C2	10nF	C6	10nF
C3	220pF	L1	4.7nH
C4	1pF	R	6Ω

**Table A.5** External Components on RF2132

Part no.	Value	Part no.	Value	Part no.	Value
C1	100pF	C7	3pF	C13	1nF
C2	11μF	C8	33pF	C14	100pF
C3	1μF	C9	100μF	L1	1.8nH
C4	1nF	C10	12pF	L2	6.8nH
C5	100pF	C11	4.3pF	L3	3.3nH
C6	100pF	C12	2.3μF	R	18K

**Table A.6** External Components on RF9936

Part no.	Value	Part no.	Value	Part no.	Value
C1	68pF	C6	1.8pF	C11	68pF
C2	60pF	C7		C12	1nF
C3	48pF	C8	220 $\mu$ F	L1	2.7nH
C4	1.8pF	C9	220 $\mu$ F	L2	6.8nH
C5	1nF	C10		L3	6.8nH
				R	

**Table A.7** External Components on RF2667

Part no.	Value	Part no.	Value	Part no.	Value
C1	10nF	C9	100pF	L1	390nH
C2	10nF	C10	100pF	L2	390nH
C3	100pF	C11	10nF	L3	330nH
C4	10nF	C12	1nF	R1	3K
C5	100pF	C13	100nF	R2	37K,10K
C6	7pF	C14	100nF		
C7	20pF	C15	100pF		
C8	10nF	C16	9.1pF		

## RF9958

## Absolute Maximum Ratings

Parameter	Rating	Unit
Supply Voltage	-0.5 to +5	V <sub>DC</sub>
Power Down Voltage (V <sub>PD</sub> )	-0.5 to V <sub>CC</sub> +0.7	V
I and Q Levels, per pin	1	V <sub>PP</sub>
LO1 Level, balanced	+3	dBm
LO2 Level, balanced	+6	dBm
Operating Ambient Temperature	-40 to +85	°C
Storage Temperature	-40 to +150	°C



Caution! ESD sensitive device.

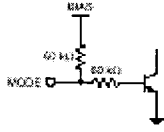
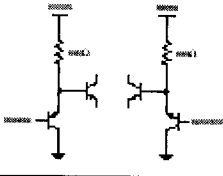
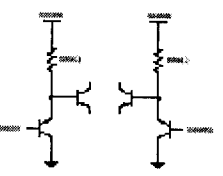
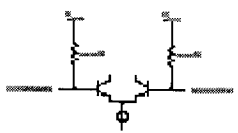
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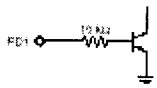
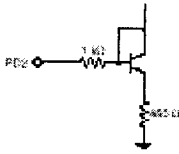
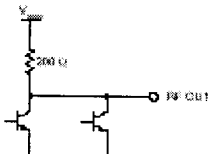
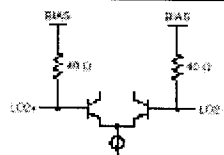
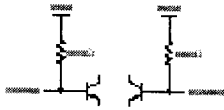
Parameter	Specification			Unit	Condition
	Min.	Typ.	Max.		
<b>I/Q Modulator &amp; AGC</b>					
I/Q Input Frequency Range		0 to 20		MHz	T=25 °C, V <sub>CC</sub> =3.0V, Z <sub>LOAD</sub> =50Ω, LO1 = -8dBm @ 260 MHz, LO2 = -3dBm @ 960 MHz, I SIG = Q SIG = 300mV <sub>PP</sub> RF Output externally matched
I/Q Input Impedance	50	80	110	kΩ	Balanced
I/Q Input Reference Level		0.6		V <sub>DC</sub>	Balanced
LO1/FM Frequency Range		240 to 360		MHz	Per Pin
LO1/FM Input Level	-15	-8	-5	dBm	
LO1/FM Input Impedance	170	200	230	Ω	Balanced
Sideband Suppression	35	40		dBc	I/Q Amplitude adjusted to within ±20mV
		30		dBc	Unadjusted
Carrier Suppression	40	50		dBc	I/Q DC Offset adjusted to within ±20mV
		30		dBc	Unadjusted
Max Output, FM Mode	+2.5	+4		dBm	V <sub>CC</sub> =2.5 V <sub>DC</sub> , T=-20°C to +85°C
Max Output, CDMA Mode	-3	0		dBm	V <sub>CC</sub> =2.5 V <sub>DC</sub> , T=-20°C to +85°C, IS-95A CDMA Modulation
		0		dBm	ISIG=QSIG=300mV <sub>PP</sub> @ 100kHz
Min Output, CDMA Mode	-2	-95	-89	dBm	V <sub>CC</sub> =0.5 V <sub>DC</sub> , T=-20°C to +85°C, IS-95A CDMA Modulation
Output Power Accuracy	-3		+3	dB	T=-20 to +85 °C, Ref=25 °C
	-2		+2	dB	1.4V ≤ GC ≤ 2.5
Adjacent Channel Power Rejection @ 885kHz		-55		dBc	IS-95A CDMA Modulation P <sub>OUT</sub> = -5dBm
Adjacent Channel Power Rejection @ 1.98MHz		-67		dBc	IS-95A CDMA Modulation P <sub>OUT</sub> = -5dBm
Output Noise Power		-116	-111	dBm/Hz	P <sub>OUT</sub> = -3 dBm, T = -20°C to +85°C
		-137	-132	dBm/Hz	P <sub>OUT</sub> = -23 dBm, T = -20°C to +85°C
		-164	-159	dBm/Hz	P <sub>OUT</sub> < -70 dBm, T = -20°C to +85°C
Output Impedance	170	200	230	Ω	Balanced
Power Dissipation			150	mW	T = -20°C to +85°C
<b>UHF Upconverter</b>					
Conversion Gain	-1	0.5		dB	Output externally matched
Noise Figure (SSB)		15		dB	
Output IP3		+14		dBm	
IF Input Impedance	170	200	230	Ω	Balanced
IF Input Frequency Range		120 to 180		MHz	
LO2 Input Impedance		50		Ω	Single Ended
LO2 Input Level	-6	-3	0	dBm	
LO2 Input Frequency Range		700 to 1100		MHz	
RF to LO2 Isolation		20		dB	

## RF9958

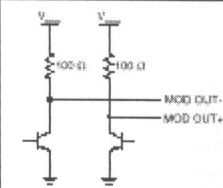
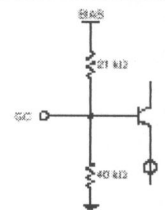
Power Supply					
Supply Voltage	2.7	3.0	3.3	V	Modulator and AGC only, CDMA Mode Mixer Only
Current Consumption		43		mA	
Current Consumption		20		mA	
Power Down Current			20	µA	
VPD HIGH Voltage	V <sub>CC</sub> -0.7			V	
VPD LOW Voltage			0.5	V	

## RF9958

Pin	Function	Description	Interface Schematic
1	MODE	Selects between CDMA and FM mode. This is a digitally controlled input. A logic "high" ( $2V_{CC} - 0.7V_{DD}$ ) selects CDMA mode. A logic "low" ( $<0.5V_{DD}$ ) selects FM mode. In FM mode, this switch enables the FM amplifier and turns off the I&Q modulator. The impedance on this pin is 30k $\Omega$ . A DC voltage less than or equal to the maximum allowable Vcc may be applied to this pin when no voltage is applied to the Vcc pins.	
2	Q SIG	Baseband input to the Q mixer. This pin is DC coupled. The DC level of 0.6V must be supplied to this pin to bias the transistor. Input impedance of this pin is 50k $\Omega$ minimum. A DC voltage less than or equal to the maximum allowable Vcc may be applied to this pin when no voltage is applied to the Vcc pins.	
3	Q REF	Reference voltage for the Q mixer. This voltage should be the same as the DC voltage supplied to the Q SIG pin. For maximum carrier suppression, DC voltage on this pin relative to the Q SIG DC voltage may be adjusted. Input impedance of this pin is 50k $\Omega$ minimum. A DC voltage less than or equal to the maximum allowable Vcc may be applied to this pin when no voltage is applied to the Vcc pins.	See pin 2.
4	I REF	Reference voltage for the I mixer. This voltage should be the same as the DC voltage supplied to the I SIG pin. For maximum carrier suppression, DC voltage on this pin relative to the I SIG DC voltage may be adjusted. Input impedance of this pin is 50k $\Omega$ minimum. A DC voltage less than or equal to the maximum allowable Vcc may be applied to this pin when no voltage is applied to the Vcc pins.	See pin 5.
5	I SIG	Baseband input to the I mixer. This pin is DC coupled. The DC level of 0.6V must be supplied to this pin to bias the transistor. Input impedance of this pin is 50k $\Omega$ minimum. A DC voltage less than or equal to the maximum allowable Vcc may be applied to this pin when no voltage is applied to the Vcc pins.	
6	GND1	Ground connection for all baseband circuits including bandgap, AGC, flip-flop, modulator and FM amp. Keep traces physically short and connect immediately to ground plane for best performance.	
7	VCC1	Supply Voltage for the LO1 flip-flop and limiting amp only. This supply is isolated to minimize the carrier leakage. A 1nF external bypass capacitor is required, and an additional 0.1 $\mu$ F will be required if no other low frequency bypass capacitors are nearby. The trace length between the pin and the bypass capacitors should be minimized. The ground side of the bypass capacitors should connect immediately to ground plane.	
8	LO1+, FM+	One half of the balanced modulator LO1 input. The other half of the input, LO1-, is AC grounded for single-ended input applications. The frequency on these pins is divided by a factor of 2, hence the carrier frequency for the modulator becomes one half of the applied frequency. The single-ended input impedance is 100 $\Omega$ (balanced is 200 $\Omega$ ). This pin is NOT internally DC blocked. An external blocking capacitor (1nF recommended) must be provided if the pin is connected to a device with DC present. When FM mode is selected, the output of the flip-flop divider circuit is switched to the AGC amplifier inputs and the modulator mixers are not used. Note that the frequency deviation input here will be reduced by a factor of two, due to the frequency divider operation.	
9	LO1-, FM-	One half of the balanced modulator LO1 input. In single-ended applications (100 $\Omega$ input impedance), this pin is AC grounded with a 1nF capacitor.	See pin 8.

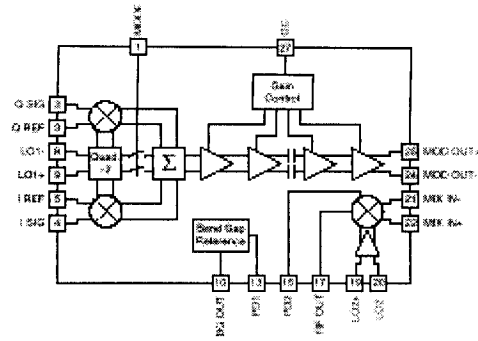
10	<b>BG OUT</b>	Bandgap voltage reference. This voltage, constant over temperature and supply variation, is used to bias internal circuits. A 1nF external bypass capacitor is required.	
11	<b>VCC3</b>	Supply voltage for the AGC and the Bandgap circuitry. A 1nF external bypass capacitor is required and an additional 0.1 $\mu$ F will be required if no other low frequency bypass capacitors are nearby. The trace length between the pin and the bypass capacitors should be minimized. The ground side of the bypass capacitors should connect immediately to ground plane.	
12	<b>GND1</b>	Same as pin 6.	
13	<b>PD1</b>	Power down control for overall circuit. When logic "high" ( $\geq V_{CC} - 0.7V$ ), all circuits are operating; when logic "low" ( $\leq 0.5V$ ), all circuits are turned off. The input impedance of this pin is $>10k\Omega$ . A DC voltage less than or equal to the maximum allowable Vcc may be applied to this pin when no voltage is applied to the Vcc pins.	
14	<b>VCC4</b>	Supply for the mixer stage only. The supply for the mixer is separated to maximize IF to RF isolations and reduce the carrier leakage. A 100pF external bypass capacitor is required and an additional 0.1 $\mu$ F will be required if no other low frequency bypass capacitors are nearby. The trace length between the pin and the bypass capacitors should be minimized. The ground side of the bypass capacitors should connect immediately to ground plane.	
15	<b>PD2</b>	Power down control for mixer only. When connected to pin 10 (BG OUT) the mixer circuits are operating; when connected to ground ( $\leq 0.5V$ ), the mixer is turned off but all other circuits are operating. A DC voltage less than or equal to the maximum allowable Vcc may be applied to this pin when no voltage is applied to the Vcc pins.	
16	<b>GND2</b>	Ground connection for the mixer stage. Keep traces physically short and connect immediately to ground plane for best performance.	
17	<b>RF OUT</b>	RF output pin. An external shunt inductor to $V_{CC}$ plus a series blocking/matching capacitor are required for 50 $\Omega$ output.	
18	<b>DEC</b>	Current Mirror decoupling pin. A 1000pF external capacitor is required to bypass this pin. The ground side of the bypass capacitors should connect immediately to ground plane.	
19	<b>LO2+</b>	One half of the balanced mixer LO2 input. In single-ended applications, the other half of the input, LO2- is AC grounded. This is a 50 $\Omega$ impedance port. This pin is NOT internally DC blocked. An external blocking capacitor (100pF recommended) must be provided if the pin is connected to a device with DC present.	
20	<b>LO2-</b>	One half of the balanced mixer LO2 input. In single-ended applications, this pin is AC grounded with a 100pF capacitor.	See pin 19.
21	<b>MIX IN-</b>	One half of the 200 $\Omega$ balanced impedance input to the mixer stage. This pin is NOT internally DC blocked. An external blocking capacitor (220pF recommended) must be provided if the pin is connected to a device with DC present. If no IF filter is needed this pin may be connected to MOD OUT+ through a DC blocking capacitor. An appropriate matching network may be needed if an IF filter is used.	
22	<b>MIX IN+</b>	Same as pin 21, except complementary input.	See pin 21.

## RF9958

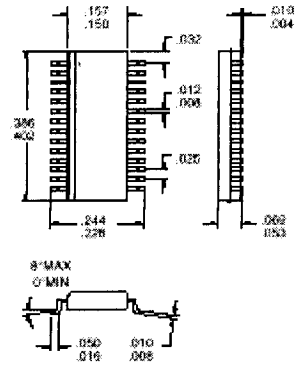
23	GND2	Same as pin 16.	
24	MOD OUT-	One half of the balanced AGC output port. The impedance of this port is 200Ω balanced. If no filtering is required, this pin can be connected to the MIX IN- pin through a DC blocking capacitor. This pin requires an inductor to V <sub>CC</sub> to achieve full dynamic range. In order to maximize gain, this inductor should be a high-Q type and should be parallel resonated out with a capacitor (see application schematic). This pin is NOT DC blocked. A blocking capacitor of 2200pF is needed when this pin is connected to a DC path. An appropriate matching network may be needed if an IF filter is used.	
25	MOD OUT+	Same as pin 24, except complementary output.	See pin 24.
26	DEC	AGC decoupling pin. An external bypass capacitor of 10nF capacitor is required. The trace length between the pin and the bypass capacitors should be minimized. The ground side of the bypass capacitors should connect immediately to ground plane.	
27	GC	Analog gain control for AGC amplifiers. Valid control voltage ranges are from 0.5V <sub>DC</sub> to 2.5V <sub>DC</sub> . The gain range for the AGC is 88dB. These voltages are valid ONLY for a 37kΩ source impedance. A DC voltage less than or equal to the maximum allowable Vcc may be applied to this pin when no voltage is applied to the Vcc pins.	
28	VCC2	Supply for the modulator stage only. A 10nF external bypass capacitor is required and an additional 0.1μF will be required if no other low frequency bypass capacitors are nearby. The trace length between the pin and the bypass capacitors should be minimized. The ground side of the bypass capacitors should connect immediately to ground plane.	

## RF9958 Pin-Out

MODE	1	28	VCC2
Q SIG	2	27	3C
Q REF	3	26	DEC
I REF	4	25	MOD OUT+
I SIG	5	24	MOD OUT-
GND1	6	23	GND2
VCC1	7	22	MIX IN+
LD1+	8	21	MIX IN-
LD1-	9	20	OC-
RG OUT	10	19	OC+
VCC3	11	18	3FC
GND1	12	17	RF OUT
PD1	13	16	GND2
VCC4	14	15	PD2



Functional Block Diagram



Package Style: SSOP-28

# RF2362

**Absolute Maximum Ratings**

Parameter	Rating	Unit
Supply Voltage	-0.5 to +8.0	V <sub>DC</sub>
Input RF Level	+10	dBm
Operating Ambient Temperature	-40 to +85	°C
Storage Temperature	-40 to +150	°C



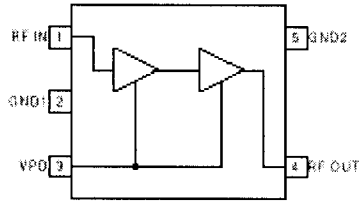
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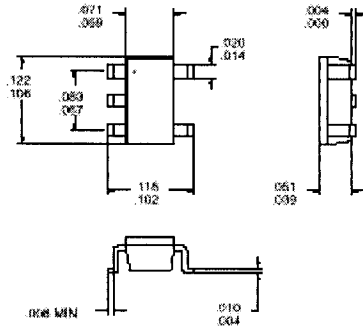
Parameter	Specification			Unit	Condition
	Min.	Typ.	Max.		
<b>Overall</b>					
RF Frequency Range		150 to 2500		MHz	
<b>1880 MHz Performance</b>					Schematic per Evaluation Board, T = 25 °C, RF = 1880 MHz, V <sub>PD</sub> = 2.8 V
Gain	19	20.1	21.5	dB	V <sub>CC</sub> = 3.5 V
	19	20.1	21.5	dB	V <sub>CC</sub> = 3.0 V
	19	20.1	21.5	dB	V <sub>CC</sub> = 2.7 V
Output IP3	+24	+25.5	+35	dBm	V <sub>CC</sub> = 3.5 V
		+25.0		dBm	V <sub>CC</sub> = 3.0 V
		+24.5		dBm	V <sub>CC</sub> = 2.7 V
Noise Figure		2.2	2.5	dB	V <sub>CC</sub> = 3.5 V
		2.2	2.5	dB	V <sub>CC</sub> = 3.0 V
		2.2	2.5	dB	V <sub>CC</sub> = 2.7 V
Reverse Isolation		32		dB	V <sub>CC</sub> = 3.5 V
		32		dB	V <sub>CC</sub> = 3.0 V
		32		dB	V <sub>CC</sub> = 2.7 V
Input VSWR		1.8:1	2.0:1		
Output VSWR		1.6:1	2.0:1		Using External LC network used on Evaluation Board
P <sub>1dB</sub>	14	14.5		dBm	V <sub>CC</sub> = 3.5 V
	12.5	14		dBm	V <sub>CC</sub> = 3.0 V
	11	13.5		dBm	V <sub>CC</sub> = 2.7 V
<b>Power Supply</b>					T = 25 °C
Voltage (V <sub>CC</sub> )		2.5 to 6.0		V	
Voltage (V <sub>PD</sub> )	2.7	2.8	2.9	V	
Current Consumption	24	35	43	mA	V <sub>CC</sub> = 3.5 V; V <sub>PD</sub> = 2.8 V; V <sub>PD</sub> + V <sub>CC</sub> - Current Consumption from V <sub>PD</sub> is 8.5 mA Typ. @ V <sub>PD</sub> = 2.8 V and 12 mA Max @ V <sub>PD</sub> = 2.9 V
	24	32	38	mA	V <sub>CC</sub> = 3.0 V; V <sub>PD</sub> = 2.7 V; V <sub>PD</sub> + V <sub>CC</sub>
	29	37	43	mA	V <sub>CC</sub> = 2.7 V; V <sub>PD</sub> = 2.9 V; V <sub>PD</sub> + V <sub>CC</sub>
- Power Down			10	µA	V <sub>CC</sub> = 3.5 V; V <sub>PD</sub> ≤ 0.9 V

# RF2362

Pin	Function	Description	Interface Schematic
1	RF IN	RF input pin. This pin is DC coupled and matched to 50Ω at 1880MHz.	
2	GND1	Ground connection. Keep traces physically short and connect immediately to ground plane for best performance.	
3	VPD	Power Down for the IC. V <sub>PD</sub> = 2.8 V +/- 0.1 V turns on the Part. V <sub>PD</sub> < 0.9 V turns off the Part. External RF bypassing is required. The trace length between the pin and the bypass capacitors should be minimized. The ground side of the bypass capacitors should connect immediately to ground plane. Nominal current required for V <sub>PD</sub> = 2.8 V is 8.5 mA typical and 12 mA Max (@ V <sub>PD</sub> = 2.9 V).	
4	RF OUT	Amplifier Output pin. This pin is an open-collector output. It must be biased to either V <sub>CC</sub> or pin 4 through a choke or matching inductor. This pin is typically matched to 50Ω with a shunt bias/matching inductor and series blocking/matching capacitor. Refer to application schematics.	
5	GND2	Ground connection. Keep traces physically short and connect immediately to ground plane for best performance.	



**Functional Block Diagram**



**Package Style: SOT23-5**

# RF2132

**Absolute Maximum Ratings**

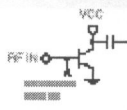
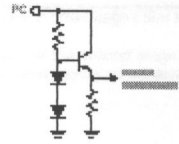
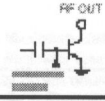
Parameter	Rating	Unit
Supply Voltage (No RF)	-0.5 to +8.0	V <sub>CC</sub>
Supply Voltage (P <sub>OUT</sub> <32dBm)	-0.5 to +6.0	V <sub>CC</sub>
Power Control Voltage (V <sub>PC</sub> )	-0.5 to +6.0 or V <sub>CC</sub>	V
DC Supply Current	800	mA
Input RF Power	+12	dBm
Output Load VSWR	10:1	
Storage Temperature	-40 to +150	°C
Junction Temperature	200	°C

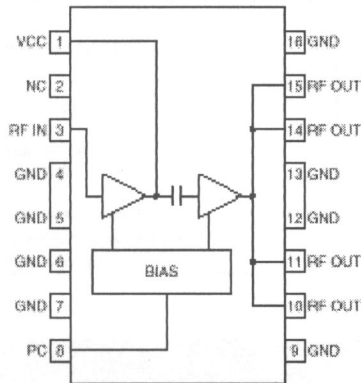


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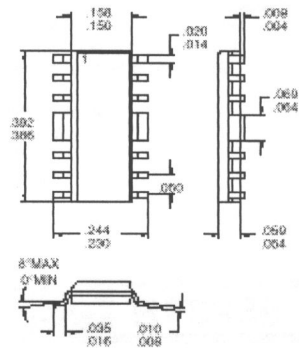
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Parameter	Specification			Unit	Condition
	Min.	Typ.	Max.		
<b>Overall</b>					T=25 °C, V <sub>CC</sub> =4.8V, V <sub>PC</sub> =4.0V, Freq=824MHz to 849MHz
Usable Frequency Range	800	824 to 849	960	MHz	
Linear Gain	27	29	31	dB	
Total Linear Efficiency	40	45		%	
Efficiency at Max Output	50	55		%	
OFF Isolation	23	27		dB	V <sub>PC</sub> =0V, P <sub>IN</sub> =+6dBm
Second Harmonic		-30		dBc	Including Second Harmonic Trap
Maximum Linear Output Power		28.5	29	dBm	IS-95A CDMA Modulation
Adjacent Channel Power Rejection @ 885 kHz		-46	-44	dBc	P <sub>out</sub> = 28 dBm ACPR can be improved by trading off efficiency.
Adjacent Channel Power Rejection @ 1.98 MHz		-58	-56	dBc	P <sub>out</sub> = 28 dBm
Maximum CW Output Power	31.5	32		dBm	
Operating Case Temperature	-30		110	°C	P <sub>out</sub> = 31 dBm, Efficiency = 55%
Ambient Operating Temperature	-30		100	°C	
Junction to Case Thermal Resistance		85		°C/W	
Input VSWR		<2:1			
Output Load VSWR			10:1		No oscillations
<b>Power Down</b>					
Turn On/Off Time			100	ns	
Total Current			10	µA	"OFF" State
V <sub>PC</sub> "OFF" Voltage	0.2		0.5	V	
V <sub>PC</sub> "ON" Voltage	3.6	4.0	V <sub>CC</sub>	V	
<b>Power Supply</b>					
Power Supply Voltage	4.2	4.8	6.0	V	Operating voltage
Idle Current		40	100	mA	V <sub>PC</sub> =4.0V
Current into VPC pin		15	20	mA	"ON" State

Pin	Function	Description	Interface Schematic
1	VCC1	Power supply for the driver stage, and interstage matching. Shunt inductance is required on this pin, which can be achieved by an inductor to $V_{CC}$ , with a decoupling capacitor on the $V_{CC}$ side. The value of the inductor is frequency dependent; 3.3nH is required for 830MHz, and 1.2nH for 960MHz. Instead of an inductor, a high impedance microstrip line can be used.	
2	NC	Not Connected.	
3	RF IN	RF input. This is a 50Ω input, but the actual input impedance depends on the interstage matching network connected to pin 1. An external DC blocking capacitor is required if this port is connected to a DC path to ground or a DC voltage.	See pin 1.
4	GND	Ground connection. Keep traces physically short and connect immediately to the ground plane for best performance.	
5	GND	Same as pin 4.	
6	GND	Ground for stage 1. Keep traces physically short and connect immediately to ground plane for best performance. This ground should be isolated from the batwing and other ground contacts. See evaluation board layout.	
7	GND	Same as pin 6.	
8	PC	Power Control. When this pin is "low", all circuits are shut off. A "low" is typically 0.5V or less at room temperature. During normal operation this pin is the power control. Control range varies from about 2V for 0dBm to $V_{CC}$ for +31 dBm RF output power. The maximum power that can be achieved depends on the actual output matching. PC should never exceed 6.0V or $V_{CC}$ , whichever is the lowest.	
9	GND	Same as pin 4.	
10	RF OUT	RF Output and power supply for the output stage. The four output pins are combined, and bias voltage for the final stage is provided through these pins. The external path must be kept symmetric until combined to ensure stability. An external matching network is required to provide the optimum load impedance; see the application schematics for details.	
11	RF OUT	Same as pin 10.	See pin 10.
12	GND	Same as pin 4.	
13	GND	Same as pin 4.	
14	RF OUT	Same as pin 10.	See pin 10.
15	RF OUT	Same as pin 10.	See pin 10.
16	GND	Same as pin 4.	



Functional Block Diagram



Package Style: SOP-16 BW

## RF9936

## Absolute Maximum Ratings

Parameter	Rating	Unit
Supply Voltage	-0.5 to 7.0	V <sub>CC</sub>
Input LO and RF Levels	+6	dBm
Ambient Operating Temperature	-40 to +85	°C
Storage Temperature	-40 to +150	°C



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
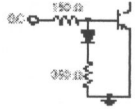
Parameter	Specification			Unit	Condition
	Min.	Typ.	Max.		
<b>Overall</b>					T = 25 °C, V <sub>CC</sub> = 3.6V, RF = 1959MHz, LO = 1749MHz @ -2dBm
RF Frequency Range		1500 to 2500		MHz	
LO Frequency Range		1200 to 2500		MHz	
IF Frequency Range		DC to 500		MHz	
<b>Cascaded Performance</b>					1kΩ balanced load, 2.5dB Image Filter Loss.
Cascade Conversion Gain, Maximum		27.5		dB	By varying the gain of the second stage, a trade-off of gain and noise figure against IP3 can be made. V <sub>G</sub> ≤ 0.5V
Cascade Conversion Gain, Minimum		15.5		dB	V <sub>G</sub> ≥ 2.5V
Cascade Input IP3		-14		dBm	Maximum Gain
Cascade Noise Figure		-9		dBm	Minimum Gain
		2.5		dB	Single sideband, at Maximum Gain Setting
		5.1		dB	Single sideband, at Minimum Gain Setting
<b>First Section (LNA)</b>					The LNA section may be left unused. Power is not connected to pin 1. The performance is then as specified for the Second Section (Mixer).
Noise Figure		1.4		dB	Input is internally matched for optimum noise figure from a 50Ω source.
Input VSWR		<2.5:1			
Input IP3		+2		dBm	IP3 may be increased 10dB by connecting pin 22 to V <sub>CC</sub> through the matching inductor. The LNA's current then increases by 10mA. Other in-between IP3 vs. I <sub>CC</sub> trade-offs may be made. See pin description for pin 20.
Gain		13.5		dB	
Reverse Isolation		23		dB	
Output VSWR		<1.5:1			
<b>Second Section (Mixer)</b>					With 1kΩ balanced load.
Noise Figure		6.5		dB	By varying the gain of the second stage, a trade-off of gain and noise figure against IP3 can be made. Please see data plots. Single Sideband, at maximum gain Single Sideband, at minimum gain
Input VSWR		13.5		dB	
Input IP3		1.5:1		dBm	At maximum gain At minimum gain
		-3		dBm	
Conversion Gain, Maximum		+2		dB	V <sub>G</sub> ≤ 0.2V
Conversion Gain, Minimum		16		dB	V <sub>G</sub> ≥ 2.5V
Output Impedance		6		kΩ	Balanced
		1			

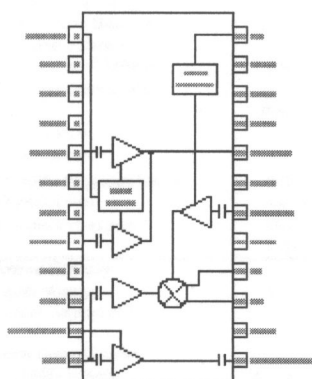
## RF9936

<b>LO Input</b>					
LO Input Range		-5 to +3		dBm	Buffer On, -2dBm input Buffer Off, -2dBm input  Single ended
LO Output Level		-5		dBm	
LO to RF (Mix In) Rejection		-25		dBm	
LO to IF1, IF2 Rejection		30		dB	
LO Input VSWR		20		dB	
<b>Power Supply</b>					
Voltage		3.6 ± 5%		V	LNA only LNA + Mixer, LO Buffer On LNA + Mixer, LO Buffer Off
Current Consumption		5		mA	
		46	50	mA	
		43	47	mA	

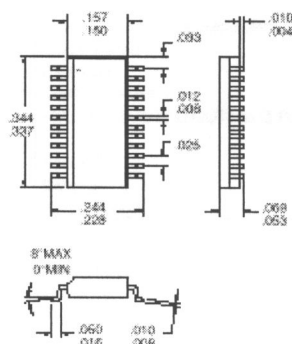
## RF9936

Pin	Function	Description	Interface Schematic
1	LNA SEL	Selects which LNA (LNA1 or LNA2) is active. This is a digitally controlled input. A logic "high" ( $\geq 3.1$ V) selects LNA2. A logic "low" ( $\leq 0.5$ V) selects LNA1.	
2	VCC1	Supply Voltage for the Mixer and RF Buffer Amplifier. External RF bypassing is required. The trace length between the pin and the bypass capacitor should be minimized. The ground side of the bypass capacitor should connect immediately to ground plane.	
3	VCC2	Supply Voltage for the LNAs and associated select logic. External RF bypassing is required. The trace length between the pin and the bypass capacitor should be minimized. The ground side of the bypass capacitor should connect immediately to ground plane.	
4	GND1	Ground connection for LNA2. Keep traces physically short and connect immediately to ground plane for best performance.	
5	LNA2 IN	RF Input pin for LNA2. This pin is internally DC blocked and internally matched for minimum noise figure (NOT for minimum VSWR), given a 50 Ω source impedance.	
6	GND2	Same as pin 4.	
7	GND3	Ground connection for LNA1. Keep traces physically short and connect immediately to ground plane for best performance.	
8	LNA1 IN	RF Input pin for LNA1. This pin is internally DC blocked and internally matched for minimum noise figure (NOT for minimum VSWR), given a 50 Ω source impedance.	
9	GND4	Same as pin 7.	
10	VCC3	Supply voltage for both LO buffer amplifiers. External RF bypassing is required. The trace length between the pin and the bypass capacitor should be minimized. The ground side of the bypass capacitor should connect immediately to ground plane.	
11	LO BUFF EN	Enable pin for the LO output buffer amplifier. This is a digitally controlled input. A logic "high" ( $\geq 3.1$ V) turns the buffer amplifier on, and the current consumption increases by 3 mA (with -2 dBm LO input). A logic "low" ( $\leq 0.5$ V) turns the buffer amplifier off.	
12	LO IN	Mixer LO Input pin. This pin is internally DC blocked and matched to 50 Ω.	
13	LO BUFF OUT	Optional Buffered LO Output. This pin is internally DC blocked and matched to 50 Ω. The buffer amplifier is switched on or off by the voltage level at pin 11.	
14	GND5	Ground connection for both LO buffer amplifiers. Keep traces physically short and connect immediately to ground plane for best performance.	
15	IF+	Open-collector IF Output pin. This is a balanced output. The output impedance is set by an internal 1000 Ω resistor to pin 16. Thus the differential IF output impedance is 1000 Ω. The resistor sets the operating impedance, but an external choke or matching inductor to $V_{CC}$ must be supplied in order to bias this output. This inductor is typically incorporated in the matching network between the output and IF filter. Because this pin is biased to $V_{CC}$ , a DC blocking capacitor must be used if the IF filter input has a DC path to ground.	
16	IF-	Same as pin 15, except complementary output.	See pin 15.
17	GND6	Ground connection for the Mixer. Keep traces physically short and connect immediately to ground plane for best performance.	
18	MIX RF IN	Mixer RF Input Pin. This pin is internally DC blocked and matched to 50 Ω.	
19	GND7	Same as pin 17.	

20	LNA OUT	LNA Output pin. This is an open-collector output. This pin is typically connected to pin 22 through a bias/matching inductor. This inductor, in conjunction with a series blocking/matching capacitor, forms a matching network to the 50Ω image filter and provides bias (see Application Example). The LNA's IP3 may be increased 10dB by connecting pin 20 to V <sub>CC</sub> through the inductor. The LNA's current then increases by 10mA. Other in-between IP3 vs. I <sub>CC</sub> trade-offs may be made by connecting resistance values between V <sub>CC</sub> and the matching inductor. The two reference points for consideration are with 150Ω used, which is what connection to pin 22 achieves, the Input IP3 is +2dBm and the LNA I <sub>CC</sub> is 5mA. Using no resistance, the Input IP3 is +12 dBm and the LNA I <sub>CC</sub> is 15 mA. Desired operating points in between these values may be interpolated, roughly.	
21	GND8	Same as pin 17.	
22	VCC4	Output supply voltage for the LNA Output (pin 20). This pin should NOT be connected to a voltage supply. This pin should be connected to pin 20 through a bias/matching inductor (see Application Example). External RF bypassing is required. The trace length between the pin and the bypass capacitor should be minimized. The ground side of the bypass capacitor should connect immediately to ground plane.	See pin 2.
23	GND9	Same as pin 17.	
24	GC	Analog gain adjustment for RF buffer amplifier. Minimum gain is selected with 2.5V to 3.0V. Maximum gain is selected with 0V to 0.5 V. When operating the RF9936 at fixed maximum gain, this pin may be grounded.	



Functional Block Diagram



Package Style: SSOP-24

**RF2667**

**Absolute Maximum Ratings**

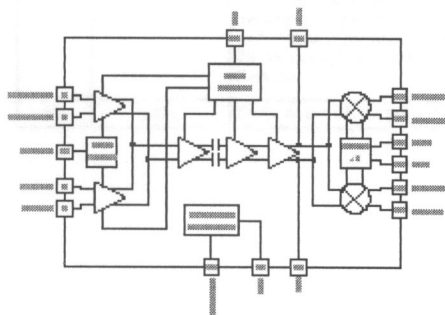
Parameter	Rating	Unit
Supply Voltage	-0.5 to +5	V <sub>CC</sub>
Power Down Voltage (V <sub>PD</sub> )	-0.5 to V <sub>CC</sub> +0.7	V <sub>CC</sub>
Input RF Power	+3	dBm
Ambient Operating Temperature	-40 to +85	°C
Storage Temperature	-40 to +150	°C



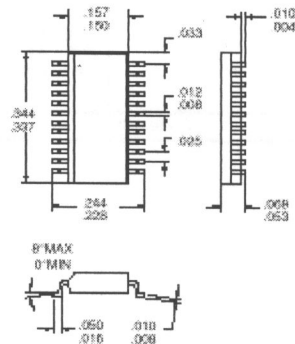
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Parameter	Specification			Unit	Condition
	Min.	Typ.	Max.		
<b>Overall (Cascaded)</b>					T=25°C, V <sub>CC</sub> =3.0V, Z <sub>LOAD</sub> =5kΩ, LO=170MHz @400mV <sub>PP</sub> IF Freq=85MHz, Z <sub>S</sub> =500Ω (CDMA), Z <sub>S</sub> =850Ω (FM)
Maximum Gain	+45	+50		dB	V <sub>CC</sub> =2.5V, FM or CDMA Input, Balanced
Minimum Gain		-55	-50	dB	V <sub>CC</sub> =0.5V, FM or CDMA Input, Balanced
Gain Variation	-3		+3	dB	T = -20°C to +85°C, Ref = 25°C
Input IP3	-54	-50		dBm	V <sub>CC</sub> =2.5V, Maximum Gain
	-7	-4		dBm	V <sub>CC</sub> =0.5V, Minimum Gain
	-39	-36		dBm	Gain = 35 dB, P <sub>avg</sub> =-61dBm
Noise Figure		5	8	dB	V <sub>CC</sub> =2.5V, Maximum Gain
		70	77	dB	V <sub>CC</sub> =0.5V, Minimum Gain
IF Input Frequency Range	50	70 to 230	300	MHz	
IF Input Impedance	2040	2400	2760	Ω	FM or CDMA, Balanced
	1020	1200	1380	Ω	FM or CDMA, Single-ended
I/Q Frequency Range	0		50	MHz	
I/Q Amplitude Balance		0.1	0.5	dB	
I/Q Phase Balance		1	5	deg	
Max I/Q Output Voltage	2.0	2.4		V <sub>PP</sub>	Balanced, maximum output level
I/Q Output Impedance	1020	1200	1380	Ω	Single-ended
	2040	2400	2760	Ω	Balanced
I/Q DC Output		2.0		V <sub>DC</sub>	Common Mode
I/Q DC Offset		20		mV <sub>DC</sub>	I OUT+ to I OUT-; Q OUT+ to Q REF-
LO Input Frequency Range	100	140 to 460	600	MHz	
LO Input Level	60	400	600	mV <sub>PP</sub>	Balanced
LO Input Impedance	680	800	920	Ω	Balanced
	340	400	460	Ω	Single Ended
<b>Power Supply</b>					
Supply Voltage	2.7	3.0	3.3	V	
Current Consumption		20	23	mA	CDMA Mode
		20	23	mA	FM Mode
Power Down Current			20	μA	
V <sub>PD</sub> HIGH Voltage	V <sub>CC</sub> -0.7			V	
V <sub>PD</sub> LOW Voltage			0.5	V	

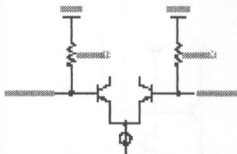
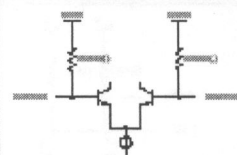
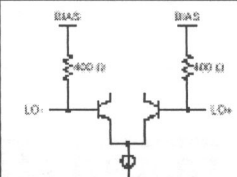


**Functional Block Diagram**



**Package Style: SSOP-24**

## RF2667

Pin	Function	Description	Interface Schematic
1	VCC1	Supply voltage for the LO flip-flop divider and limiting amp. This pin may be connected in parallel with pins 2 and 3. It should be bypassed by a 10nF capacitor. The trace length between the pin and the bypass capacitor should be minimized. The ground side of the bypass capacitor should connect immediately to ground plane. The part is designed to work from a 2.7V to 3.3V supply.	
2	VCC2	Supply voltage for the bandgap, gain control bias circuitry, and AGC stages 2, 3, and 4. This pin may be connected in parallel with pins 1 and 3. It should be bypassed by a 10nF capacitor. The trace length between the pin and the bypass capacitor should be minimized. The ground side of the bypass capacitor should connect immediately to ground plane. The part is designed to work from a 2.7V to 3.3V supply.	
3	VCC3	Supply voltage for the FM and CDMA AGC input stages. This pin may be connected in parallel with pins 1 and 2. It should be bypassed by a 10nF capacitor. The trace length between the pin and the bypass capacitor should be minimized. The ground side of the bypass capacitor should connect immediately to ground plane. The part is designed to work from a 2.7V to 3.3V supply.	
4	CDMA IN+	CDMA Balanced Input pin. This pin is internally DC biased and should be DC blocked if connected to a device with a DC level present. For single-ended input operation, one pin is used as an input and the other CDMA input is AC coupled to ground. The balanced input impedance is 2.4k $\Omega$ , while the single-ended input impedance is 1.2k $\Omega$ .	
5	CDMA IN-	Same as pin 4, except complementary input.	See pin 4.
6	GND	Ground connection. Keep traces physically short and connect immediately to ground plane for best performance.	
7	GND	Same as pin 6.	
8	FM IN+	FM Balanced Input pin. This pin is internally DC biased and should be DC blocked if connected to a device with DC present. For single-ended input operation, one pin is used as an input and the other FM input is AC coupled to ground. The balanced input impedance is 2.4k $\Omega$ , while the single-ended input impedance is 1.2k $\Omega$ .	
9	FM IN-	Same as pin 8, except complementary input.	See pin 8.
10	BG OUT	Bandgap Voltage Reference. This voltage, constant over temperature and supply variation, is used to bias internal circuits. A 10nF external bypass capacitor is required. The trace length between the pin and the bypass capacitor should be minimized. The ground side of the bypass capacitor should connect immediately to ground plane.	
11	DEC	AGC decoupling pin. An external bypass capacitor of 10nF capacitor is required. The trace length between the pin and the bypass capacitor should be minimized. The ground side of the bypass capacitor should connect immediately to ground plane.	
12	LO-	LO Balanced Input pin. This pin is internally DC biased and should be DC blocked if connected to a device with DC present. For single-ended input operation, one pin is used as an input and the other LO input is AC coupled to ground. The frequency of the signal applied to these pins is internally divided by a factor of 2, hence the carrier frequency for the modulator becomes one half of the applied frequency. The single-ended input impedance is 400 $\Omega$ (balanced is 800 $\Omega$ ). The LO input may be driven single-ended but balanced provides optimum gain and phase balance.	
13	LO+	Same as pin 12, except complementary input.	See pin 12.

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Pin	Function	Description	Interface Schematic
14	IN SEL	Selects between CDMA and FM mode. This is a digitally controlled input. A logic "high" ( $\geq V_{CC} - 0.7V_{DC}$ ) selects CDMA mode. A logic "low" ( $< 0.5V_{DC}$ ) selects FM mode. The impedance on this pin is 30k $\Omega$ .	
15	Q OUT-	Balanced Baseband Output of Q Mixer. This pin is internally DC biased and should be DC blocked externally. This output is active in both CDMA and FM modes. The output can be used in a single-ended configuration by leaving one of the two pins unconnected, however half the output voltage will be lost. Each pin should be loaded with 2.5k $\Omega$ . The balanced load should be 5k $\Omega$ . The single-ended output impedance is 1.2k $\Omega$ , while the balanced output impedance is 2.4k $\Omega$ .	
16	Q OUT+	Same as pin 15, except complementary output.	See pin 15.
17	GND	Same as pin 6.	
18	FL-	Balanced AGC Output/Demod Input. This balanced node is pinned out to allow shunt filtering of the AGC output signal as it enters the demodulator. The basic configuration of the filter should consist of a shunt inductor and shunt capacitor, both connected to the power supply, as the internal circuitry requires this power supply connection through the inductor to operate.	
19	FL+	Same as pin 18, except complementary.	See pin 18.
20	GND	Same as pin 6.	
21	I OUT+	Balanced Baseband Output of I Mixer. This pin is internally DC biased and should be DC blocked externally. This output is active in both CDMA and FM modes. The output can be used in a single-ended configuration by leaving one of the two pins unconnected, however half the output voltage will be lost. Each pin should be loaded with 2.5k $\Omega$ . The balanced load should be 5k $\Omega$ . The single-ended output impedance is 1.2k $\Omega$ , while the balanced output impedance is 2.4k $\Omega$ .	
22	I OUT-	Same as pin 21, except complementary output.	See pin 22.
23	GC	Analog Gain Control for AGC Amplifiers. The valid control range is from 0.5 to 2.5V $_{DC}$ . These voltages are valid for ONLY a 37k $\Omega$ source impedance. The gain range for the AGC is 95dB.	

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Pin	Function	Description	Interface Schematic
24	PD	Power Down Control. When logic "high" ( $\geq V_{CC} - 0.3V$ ), all circuits are operating; when logic "low" ( $\leq 0.5V$ ), all circuits are turned off. The input impedance of this pin is 10k $\Omega$ .	