

**DIGITAL CONTROL OF AN
ENCRYPTIC BROAD-BAND
RADAR APPLICATION**

BY

VIJAYA SRINIVASA RAGHAVAN

A DISSERTATION SUBMITTED TO THE
UNIVERSITY OF ZAMBIA IN
FULFILMENT OF THE REQUIREMENTS
OF THE DEGREE OF MASTER IN
ENGINEERING

256038

THE UNIVERSITY OF ZAMBIA
LUSAKA

1998

I, Vijaya Srinivasa Raghavan, hereby solemnly declare that this thesis represents my own work and that to my knowledge it has not previously been submitted for a degree at this or any other university.



Vijaya Srinivasa Raghavan

Date: 27th March, 1998.

DECLARATION

I, Vijaya Srinivasa Raghavan, hereby solemnly declare that this thesis represents my own work and that to my knowledge it has not previously been submitted for a degree at this or any other university.



Vijaya Srinivasa Raghavan

Date: 27th March, 1998.

This dissertation of Vijaya Srinivasa Raghavan is approved as fulfilling the requirements for the award of the Degree of Master of Engineering (Electrical and Electronics) by the University of Zambia.

Examiner's Signature

Date

1. 

17th April 1990

2. _____

3. _____

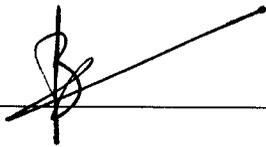
4. _____

APPROVAL

This dissertation of Vijaya Srinivasa Raghavan is approved as fulfilling the requirements for the award of the Degree of Master of Engineering (Electrical and Electronics) by the University of Zambia.

Examiner's Signature

Date

1.  _____

17th April 1990

2. _____

3. _____

4. _____

This project describes the digital control of a radar that is ideally insensitive to alien disturbance signals. The key factor in this project comprises the design and realisation of a wide range of digital techniques combined into one digital controller consisting of several elements.

The project is divided into three major parts, namely,

Transmitter, Channel and Receiver.

Transmitter:

A radar control circuitry that generates binary noise with hidden codes has been developed. A modulo-2 feedback shift register generates a pseudo-random sequence. This sequence constitutes the binary noise. The codes [called Complementary Semi-Barker codes] are generated by cascading 16-1 multiplexers. Control signals were developed to establish a switch. The output of this switch transmits a signal consisting of the noise and the codes. The codes are known only to the sender. This makes it difficult for an intelligent target to distinguish between the codes and the binary noise. Consequently, this radar system is hard to influence.

Receiver:

The codes are matched using auto-correlation technique. In order to retrieve the matched codes, they have to appear in an adder simultaneously. This calls for the introduction of a delay in the signal. A threshold voltage is set to clip off the undesired part of the retrieved signal. This resembles a traditional radar signal.

ABSTRACT

This project describes the digital control of a radar that is ideally insensitive to alien disturbance signals. The key factor in this project comprises the design and realisation of a wide range of digital techniques combined into one digital controller consisting of several elements.

The project is divided into three major parts, namely,
Transmitter, Channel and Receiver.

Transmitter:

A radar control circuitry that generates binary noise with hidden codes has been developed. A modulo-2 feedback shift register generates a pseudo-random sequence. This sequence constitutes the binary noise. The codes [called Complementary Semi-Barker codes] are generated by cascading 16-1 multiplexers. Control signals were developed to establish a switch. The output of this switch transmits a signal consisting of the noise and the codes. The codes are known only to the sender. This makes it difficult for an intelligent target to distinguish between the codes and the binary noise. Consequently, this radar system is hard to influence.

Receiver:

The codes are matched using auto-correlation technique. In order to retrieve the matched codes, they have to appear in an adder simultaneously. This calls for the introduction of a delay in the signal. A threshold voltage is set to clip off the undesired part of the retrieved signal. This resembles a traditional radar signal.

Channel:

A channel is introduced in the final stage to intrude on the output of the transmitter. Disturbances in the form of additional pulses are introduced in order to investigate the sensitivity and robustness of the encryption technique.

I wish to thank a number of people who are behind the success of my project. I first thank the Head, Department of Electrical and Electronic Engineering. I also wish to thank my guides, Mr. D. Beekman and Prof. J.M. Mwenechanya for all the encouragement and guidance given to me. I am grateful to Mr. Sijamba for his ideas. My thanks also goes to all the members of the staff who were kind enough to assist me. Most of all I wish to thank my family and friends for their moral support and motivation not only throughout my project, but over my entire academic life.

ACKNOWLEDGEMENT

I wish to thank a number of people who are behind the success of my project. I first thank the Head, Department of Electrical and Electronic Engineering. I also wish to thank my guides, Mr. D. Beekman and Prof. J.M. Mwenechanya for all the encouragement and guidance given to me. I am grateful to Mr. Sijamba for his ideas. My thanks also goes to all the members of the staff who were kind enough to assist me. Most of all I wish to thank my family and friends for their moral support and motivation not only throughout my project, but over my entire academic life.

Contents	Page No.
DECLARATION	ii
APPROVAL	iii
ABSTRACT	iv
ACKNOWLEDGEMENTS	vi
TABLE OF CONTENTS	vii
LIST OF TABLES	ix
LIST OF FIGURES	x
1. INTRODUCTION	1-4
1.1. Brief history	1
1.2. Aim of the project	2
2. LITERATURE	5-17
2.1. Counters	5
2.2. One-shots	8
2.3. Multiplexers	10
2.4. Operational amplifiers as adders	12
2.5. Maximum length sequences	13
2.6. Complementary Semi-Barker codes and Matched filters	14
2.7. Clipping circuits	17
3. TRANSMITTER	18-25
3.1. Introduction	18

TABLE OF CONTENTS

Contents	Page No.
DECLARATION	ii
APPROVAL	iii
ABSTRACT	iv
ACKNOWLEDGEMENTS	vi
TABLE OF CONTENTS	vii
LIST OF TABLES	ix
LIST OF FIGURES	x
1. INTRODUCTION	1-4
1.1. Brief history	1
1.2. Aim of the project	2
2. LITERATURE	5-17
2.1. Counters	5
2.2. One-shots	8
2.3. Multiplexers	10
2.4. Operational amplifiers as adders	12
2.5. Maximum length sequences	13
2.6. Complementary Semi-Barker codes and Matched filters	14
2.7. Clipping circuits	17
3. TRANSMITTER	18-25
3.1. Introduction	18
3.2. Generation of noise	19
3.3. Generation of codes	20
3.4. Control signals	22

3.5.	Switch	24
3.6.	Discussion	26
4.	RECEIVER	27-35
4.1.	Introduction	27
4.2.	Auto correlation filters	28
4.3.	Delay and Adders	29
4.4.	Setting a threshold level	34
4.5.	Discussion	35
5.	CHANNEL	36-39
5.1.	Introduction	36
5.2.	Addition of disturbance to the output of the transmitter	37
5.3.	Discussion	39
6.	CONCLUSION	40
7.	REFERENCES	42
8.	GLOSSARY	43
9.	APPENDICES	45-48
	A. List of ICs, test equipment and other components used	45
	B. Example to show the working of a modulo-2 feedback shift register	46
	C. A program in Q-BASIC to determine the feedback sections in a 16 bit shift register	48

<i>Table 2.1 Logic truth table of a mod-16 counter using IC7493</i>	<i>7</i>
<i>Table 2.2 Logic table to show the working of IC74150</i>	<i>10</i>
<i>Table 2.3 Tables to show working of an auto-correlation filter</i>	<i>16</i>
<i>Table 4.1 Voltage values as the codes shift in and out of their respective filters</i>	<i>31</i>
<i>Table 5.1 Table showing effect of disturbance on the detected pulses</i>	<i>38</i>

LIST OF TABLES

Table 2.1 <i>Logic truth table of a mod-16 counter using IC7493</i>	7
Table 2.2 <i>Logic table to show the working of IC74150</i>	10
Table 2.3 <i>Tables to show working of an auto-correlation filter</i>	16
Table 4.1 <i>Voltage values as the codes shift in and out of their respective filters</i>	31
Table 5.1 <i>Table showing effect of disturbance on the detected pulses</i>	38

Figure 1.1 <i>Traditional radar signal</i>	1
Figure 1.2 <i>Outline of the project</i>	2
Figure 1.3 <i>Schematic of the project</i>	3
Figure 1.4 <i>The expected outputs at the transmitter, the channel and the receiver</i>	4
Figure 2.1 <i>Pin-out diagram of IC7493</i>	6
Figure 2.2 <i>Pin-out diagram of IC74121</i>	8
Figure 2.3 <i>Op-amp as an adder</i>	12
Figure 2.4 <i>Pin-out diagram of IC741</i>	12
Figure 2.5 <i>Modulo-2 feedback shift register</i>	13
Figure 2.6 <i>Auto-correlation filter [matched to the code, 1101]</i>	15
Figure 2.7 <i>Biased diode clipping circuit</i>	17
Figure 3.1 <i>Generation of the codes</i>	21
Figure 3.2 <i>Transmitter control signals</i>	23
Figure 3.3 <i>Switch</i>	24
Figure 3.4 <i>Detailed diagram of the entire transmitter</i>	25
Figure 3.5 <i>Solution for fan-out</i>	26
Figure 4.1 <i>Detailed diagram of the receiver</i>	29
Figure 4.2 <i>Outputs at the receiver</i>	33
Figure 4.3 <i>Biased diode clipper circuit to set the desired threshold level</i>	34
Figure 4.4 <i>Detected pulses</i>	34
Figure 5.1 <i>Introduction of disturbance in the original signal</i>	37

LIST OF FIGURES

Figure 1.1 <i>Traditional radar signal</i>	1
Figure 1.2 <i>Outline of the project</i>	2
Figure 1.3 <i>Schematic of the project</i>	3
Figure 1.4 <i>The expected outputs at the transmitter, the channel and the receiver</i>	4
Figure 2.1 <i>Pin-out diagram of IC7493</i>	6
Figure 2.2 <i>Pin-out diagram of IC74121</i>	8
Figure 2.3 <i>Op-amp as an adder</i>	12
Figure 2.4 <i>Pin-out diagram of IC741</i>	12
Figure 2.5 <i>Modulo-2 feedback shift register</i>	13
Figure 2.6 <i>Auto-correlation filter [matched to the code, 1101]</i>	15
Figure 2.7 <i>Biased diode clipping circuit</i>	17
Figure 3.1 <i>Generation of the codes</i>	21
Figure 3.2 <i>Transmitter control signals</i>	23
Figure 3.3 <i>Switch</i>	24
Figure 3.4 <i>Detailed diagram of the entire transmitter</i>	25
Figure 3.5 <i>Solution for fan-out</i>	26
Figure 4.1 <i>Detailed diagram of the receiver</i>	29
Figure 4.2 <i>Outputs at the receiver</i>	33
Figure 4.3 <i>Biased diode clipper circuit to set the desired threshold level</i>	34
Figure 4.4 <i>Detected pulses</i>	34
Figure 5.1 <i>Introduction of disturbance in the original signal</i>	37
Figure 5.2 <i>Addition of pulses via a NAND gate</i>	39
Figure. 9.1 <i>Modulo-2 feedback addition of a 4-section shift register</i>	46

1.1 Brief history

Since the introduction of the early radar at the outbreak of World War II, a lot has changed in this field. Digital techniques have over-ruled traditional analog equipment to a large extent during the last two decades. Some reasons for that are better and more constant accuracy, better reproducibility, interfacing to more computers and networks, less maintenance, lower production costs, less power consumption and an on-going increase in performance.

The essential basics of radar transmission, that is, transmitting well-defined electromagnetic energy in order to locate target positions out of echoed signals, are still valid. Counter-measures have been developed to a large extent in military applications. Potential targets try to hide behind self produced clouds of reflecting material or by intentionally misleading the radar installation by transmitting false echo-signals.

Traditional radar systems send equidistant pulses [figure 1.1] and on the reception of their echoes, the position of the targets can be determined. Intelligent targets can disturb the pulses by inserting extra echoes in-between the natural ones thereby giving "false alarms" and wrong position detection. This is an undesired situation.



Figure 1.1 Traditional radar signal

This project develops a system that transmits the signal as binary noise. Suitable codes embedded in this noise are detected at the receiver and made to resemble the traditional

1. INTRODUCTION

1.1 Brief history

Since the introduction of the early radar at the outbreak of World War II, a lot has changed in this field. Digital techniques have over-ruled traditional analog equipment to a large extent during the last two decades. Some reasons for that are better and more constant accuracy, better reproducibility, interfacing to more computers and networks, less maintenance, lower production costs, less power consumption and an on-going increase in performance.

The essential basics of radar transmission, that is, transmitting well-defined electromagnetic energy in order to locate target positions out of echoed signals, are still valid. Counter-measures have been developed to a large extent in military applications. Potential targets try to hide behind self produced clouds of reflecting material or by intentionally misleading the radar installation by transmitting false echo-signals.

Traditional radar systems send equidistant pulses [figure 1.1] and on the reception of their echoes, the position of the targets can be determined. Intelligent targets can disturb the pulses by inserting extra echoes in-between the natural ones thereby giving “false alarms” and wrong position detection. This is an undesired situation.



Figure 1.1 *Traditional radar signal*

This project develops a system that transmits the signal as binary noise. Suitable codes embedded in this noise are detected at the receiver and made to resemble the traditional radar signal.

1.2 Aim of the project

The project is about transmitting electromagnetic radar energy in the form of binary noise rather than the traditional pulses. The advantage of this non-conventional method is that intelligent targets cannot very easily influence the radar echo as can be done in the traditional way.

The project involves designing, building and testing a prototype to fulfil all the above requirements. Considering all the above stipulations, we can divide the project into three major parts, namely,

Transmitter, Channel and Receiver [figure 1.2].

In short, we have:



Figure 1.2 *Outline of the project*

A thorough schematic of figure 1.2 can be seen in figure 1.3, each part of which will be discussed in detail in the ensuing sections.

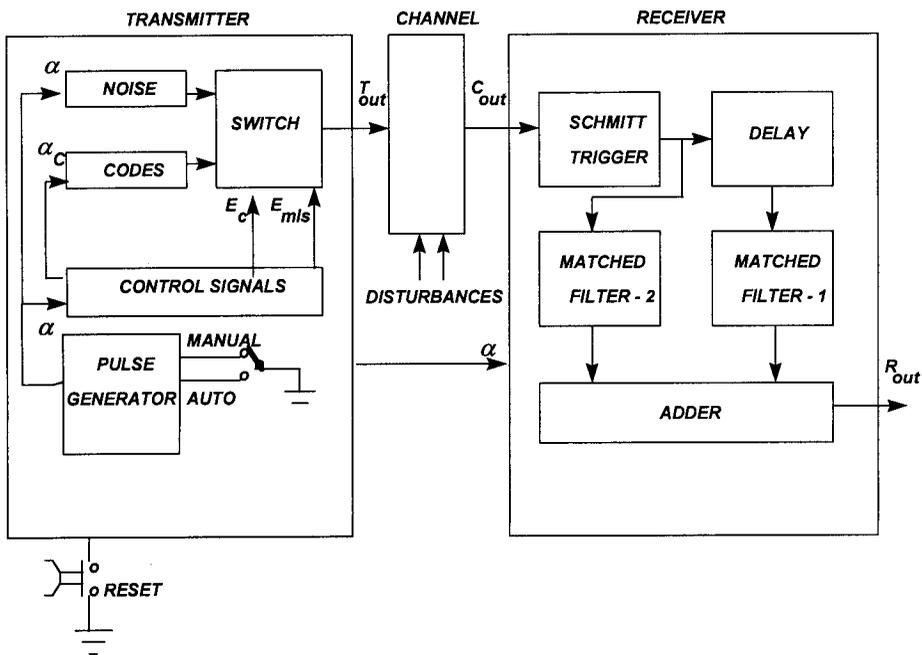


Figure 1.3 Schematic of the project

α :Clock to the system

α_c :Clock to the codes

E_{mls} :Enable signal for the maximum length sequence (noise)

E_c :Enable signal for codes

T_{out} :Output of the transmitter

C_{out} :Output of the channel

R_{out} :Output of the receiver

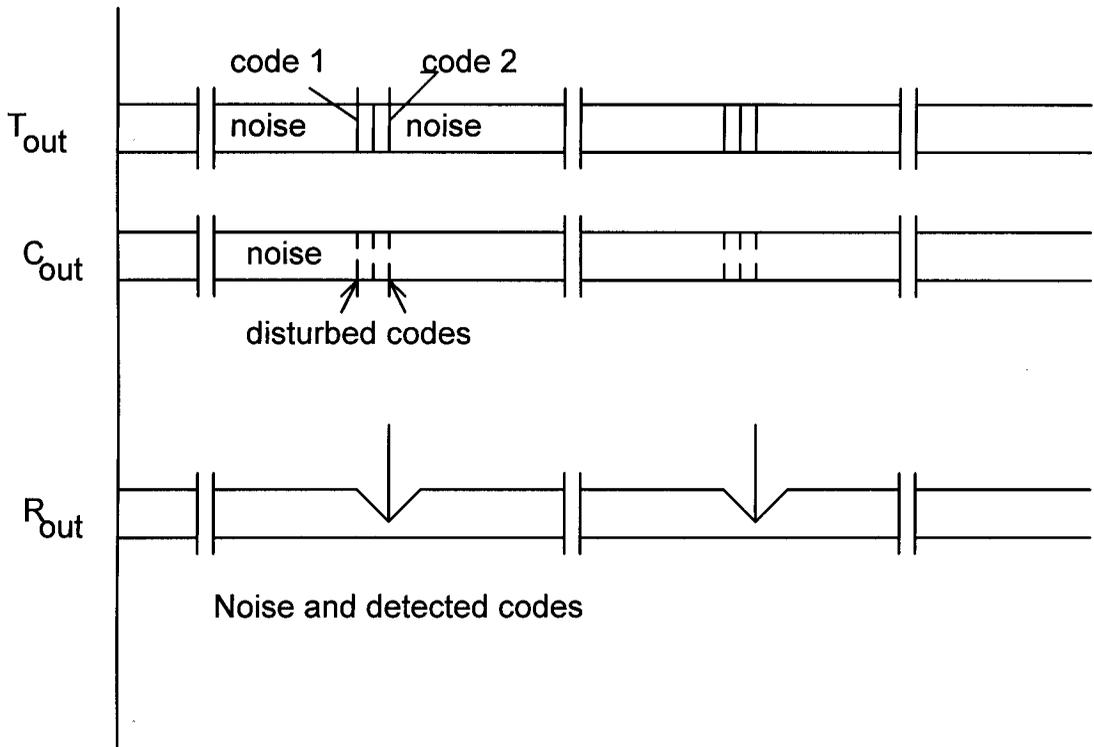


Figure 1.4 *The expected outputs at the transmitter, the channel and the receiver*

Notice that the codes are embedded in the noise at the output of the transmitter. When some alien pulses are added, the signal is expected to become unsteady. But this effect is more conspicuous in the codes. A sharp pulse at the instant both the codes appear is expected and, despite the influence of the alien signal, it [the pulse] is expected to be distinct.

2.1 Counters

A counter [5] is probably one of the most useful and versatile sub-systems in a digital system. A counter driven by a clock can be used to count the number of clock cycles. Since the clock pulses occur at known intervals, the counter can be used as an instrument for measuring time and therefore period or frequency.

A counter is constructed by connecting flip-flops in cascade. The largest binary number that can be represented by N cascaded flip-flops has a decimal equivalent of $2^N - 1$. For example, a three-flip-flop counter reaches a maximum decimal number of $2^3 - 1 = 7$. A three-flip-flop counter is referred to as a modulus-8 (or mod-8) counter since it has eight states.

The modulus of a counter is the total number of states through which it can progress.

The counter used in this project is from the 74L93 series. A number of these can be cascaded in turn to result in larger counters. Figure 2.1 is the DIP pin-out of a 7493 counter.

2. LITERATURE

2.1 Counters

A counter [5] is probably one of the most useful and versatile sub-systems in a digital system. A counter driven by a clock can be used to count the number of clock cycles. Since the clock pulses occur at known intervals, the counter can be used as an instrument for measuring time and therefore period or frequency.

A counter is constructed by connecting flip-flops in cascade. The largest binary number that can be represented by N cascaded flip-flops has a decimal equivalent of $2^n - 1$. For example, a three-flip-flop counter reaches a maximum decimal number of $2^3 - 1 = 7$. A three-flip-flop counter is referred to as a modulus-8 [or mod-8] counter since it has eight states.

The modulus of a counter is the total number of states through which it can progress.

The counter used in this project is from the 74L93 series. A number of these can be cascaded in turn to result in larger counters. Figure 2.1 is the DIP pin-out of a 7493 counter.

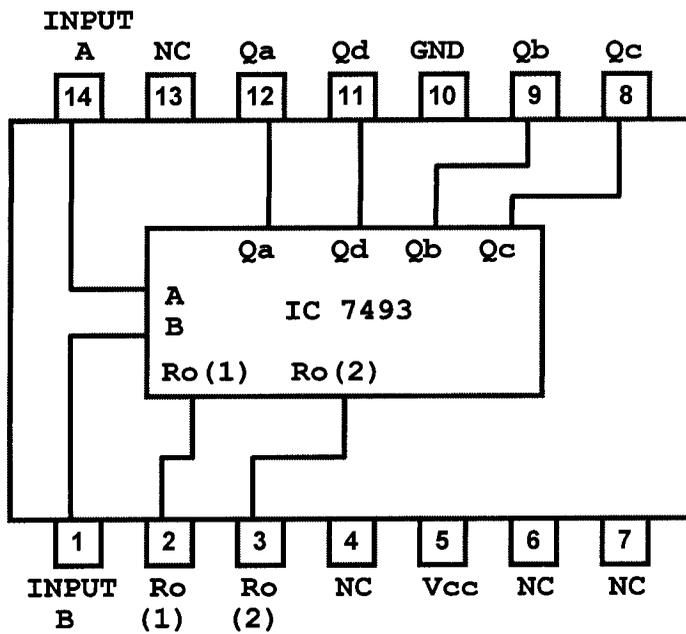


Figure 2.1 Pin-out diagram of IC7493

This TTL circuit is a 4-bit binary counter that can be used in either a mod-8 or mod-16 configuration. If the clock is applied at input B, it can be used as a mod-8 counter and if it is applied at input A, it can be used as a mod-16 counter. The truth table for a mod-16 counter can be seen in table 2.1. All the flip-flops have direct reset inputs that are active low.

Count	Qa	Qb	Qc	Qd
0	L	L	L	L
1	L	L	L	H
2	L	L	H	L
3	L	L	H	H
4	L	H	L	L
5	L	H	L	H
6	L	H	H	L
7	L	H	H	H
8	H	L	L	L
9	H	L	L	H
10	H	L	H	L
11	H	L	H	H
12	H	H	L	L
13	H	H	L	H
14	H	H	H	L
15	H	H	H	H

Table 2.1 Logic truth table of a mod-16 counter using IC7493

H => High state

L => Low state

The project uses cascaded 7493 counters in mod-512 and mod 32 configurations. These two counters are required to transmit a signal consisting of binary noise and binary codes in a period of 512 clock cycles. The codes are transmitted for 32 clock cycles and the noise for the remaining 480 cycles.

The counters are also used to control the multiplexers [chapter 2.3]. Two 7493 counters are cascaded to give a mod-32 counter. The first four outputs are used as the control inputs and the last output is used as the strobe input. Depending on whether the strobe is high or low, only one of the multiplexers is active.

2.2 One-shots

Circuits that have one stable state and one quasi-stable state are called switching circuits or one-shots [5]. The normal mode of operation is to trigger the circuit into its quasi-stable state, where it will remain for a predetermined length of time. The circuit will then switch itself back to its stable state, where it will remain until it receives another input trigger pulse. The one-shot used is the TTL 74121. Figure 2.2 shows the pin-out diagram.

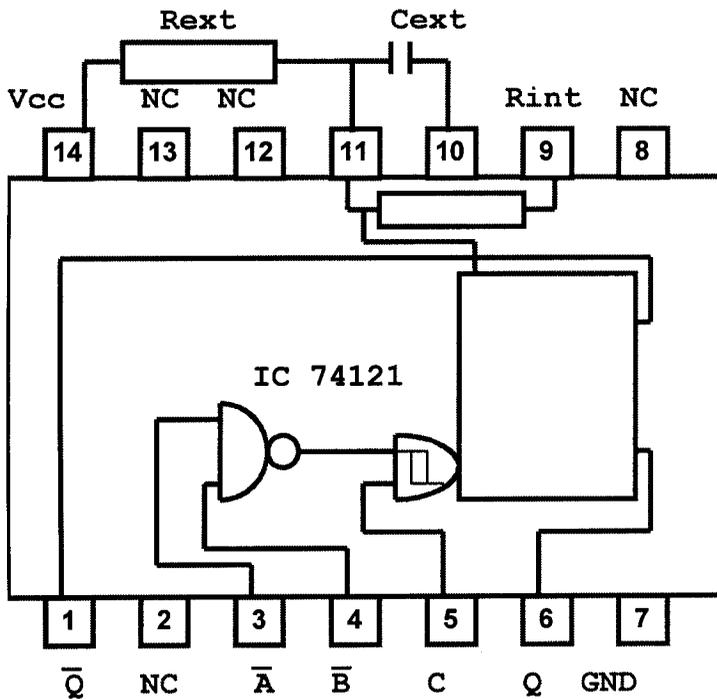


Figure 2.2 Pin-out diagram of IC74121

The inputs are \bar{A} , \bar{B} and C . The trigger input to the one-shot appears at the output of the AND gate. Here's how the gates work:

1. If C is held high, a negative transition at either \bar{A} or \bar{B} will trigger the circuit.

If either \bar{A} or \bar{B} , or both are held low, a positive transition at C will trigger the circuit.

The output pulse width at Q is set according to the values of the timing resistor R_{ext} and capacitor C_{ext} as

$$t = 0.69R_{\text{ext}}C_{\text{ext}}$$

One-shots are used in two sections, the transmitter [control signals] and the channel [disturbance].

In the control signals, the negative output of the one-shot clears the output of the Enable flip-flop. That is, every time the output, E_c goes high, it is reset after 32 clock cycles.

This gives a signal that is high for 480 clock cycles and low for 32 clock cycles.

In the channel, the positive output of the one-shot is mixed with the transmitted signal to create a disturbance.

2.3 Multiplexers

A multiplexer [5] is a circuit with many inputs and one output. By applying control signals, any input can be steered to the output. It is also called a data selector because the output bit depends on the data bit that is selected. The input bits are labelled D_0 to D_{15} . Only one of these is transmitted to the output. The control nibble determines which of the input data bits is transmitted to the output. The complement of the selected data bit, rather than the data itself, is obtained.

$Y = \overline{D}_n$ [Table 2.2], where n is the decimal equivalent of the control signal ABCD. A

high strobe disables the multiplexer and forces the output into the high state. With a high strobe, the value of ABCD does not matter. The action of a multiplexer can be understood by studying table 2.2.

DATA	A	B	C	D	STROBE	Y
D ₀	0	0	0	0	0	\overline{D}_0
D ₁	0	0	0	1	0	\overline{D}_1
D ₂	0	0	1	0	0	\overline{D}_2
D ₃	0	0	1	1	0	\overline{D}_3
D ₄	0	1	0	0	0	\overline{D}_4
D ₅	0	1	0	1	0	\overline{D}_5
D ₆	0	1	1	0	0	\overline{D}_6
D ₇	0	1	1	1	0	\overline{D}_7
D ₈	1	0	0	0	0	\overline{D}_8
D ₉	1	0	0	1	0	\overline{D}_9
D ₁₀	1	0	1	0	0	\overline{D}_{10}
D ₁₁	1	0	1	1	0	\overline{D}_{11}
D ₁₂	1	1	0	0	0	\overline{D}_{12}
D ₁₃	1	1	0	1	0	\overline{D}_{13}
D ₁₄	1	1	1	0	0	\overline{D}_{14}
D ₁₅	1	1	1	1	0	\overline{D}_{15}
X	X	X	X	X	1	1

Table 2.2 Logic table to show the working of IC74150

The last column is the complement of the output, Y' and not the output itself. "X" implies that the value of the data input or the control inputs does not matter when the strobe is high.

The project uses a pair of Complementary Semi-Barker codes [4]. These codes are generated by cascading two 16-1 multiplexers. A multiplexer has data inputs [which are connected with respect to the codes], control inputs and a strobe input. The control and data inputs are the outputs of a mod-32 counter [Chapter 2.1]. Table 2.2 shows that when the strobe is high, the data is always high, irrespective of the other inputs. Since there are two codes of length 16 bits each and two multiplexers to generate them, the strobe is made high for 16 clock cycles and low for another 16 clock cycles. By doing this, only one of the two multiplexers is active at an instant. The data present in the active multiplexer is generated as output.

2.4 Operational amplifiers as adders

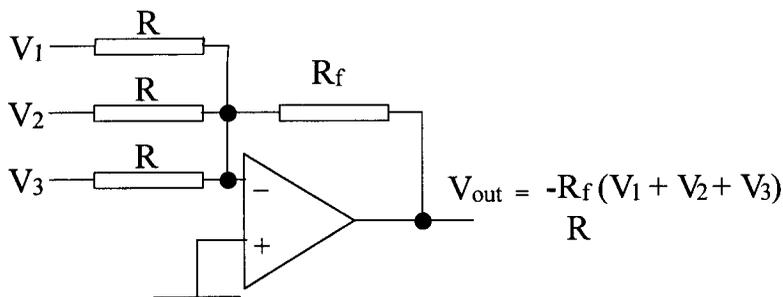


Figure 2.3 Op-amp as an adder

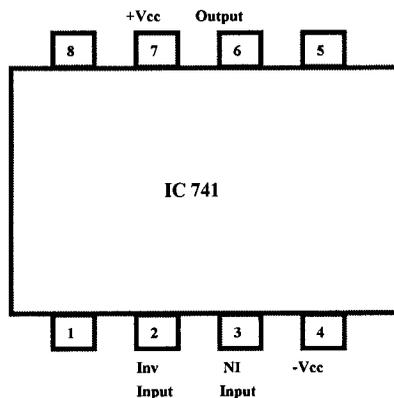


Figure 2.4 Pin-out diagram of IC741

An operational amplifier is a circuit which is chiefly used for mathematical operations. When it is used as an adder, the voltages are applied to the inverting (INV) input terminal via resistors. The Non-inverting input is connected to ground. By varying the feedback resistor, the amplification factor of the output voltage can be adjusted.

The op-amps are used in the receiver to add the outputs of the matched filters. The matched outputs of the two filters are fed to the INV inputs of two op-amps via resistors. The outputs of the two filters are in turn added. Every time the two codes are simultaneously present in their respective filters, the output of the last op-amp is expected to be maximum. This maximum voltage indicates the presence of codes.

2.5 Maximum length sequences

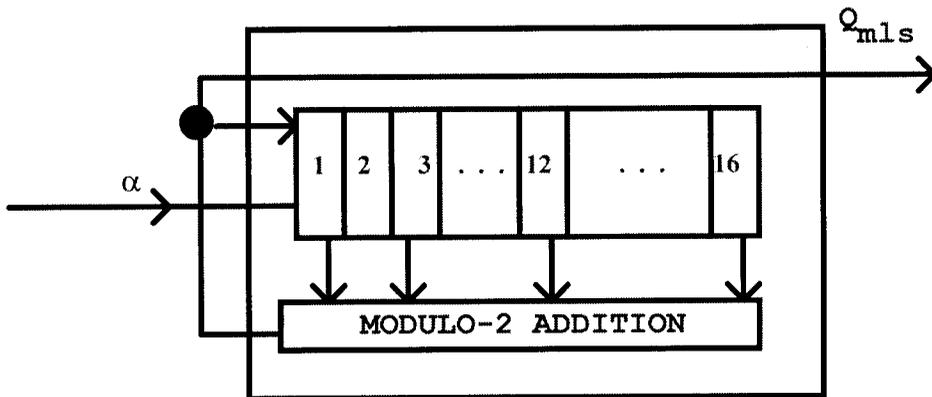


Figure 2.5 Modulo-2 feedback shift register

When certain pre-determined sections of a shift register are combined for mod-2 addition and the resultant is fed back to the first section we get a pseudo-random sequence [figure 2.5]. Each stage uniquely determines its following stage, making the sequence pseudo-random. With proper feedback, a shift register with “k” sections, can result in two possible sets of outputs depending on the initial input. If it consists of only zeroes, the output will be a zero sequence of length 1. For any other initial input, there can be as many as $2^k - 1$ outputs and is called a maximum length sequence [2].

In this project the above concept is used to generate a maximum length sequence from a 16-bit shift register to represent binary noise. The task of obtaining the necessary feedback combination can be tedious when done manually. A program in Q-BASIC was developed to handle this.

2.6 Complementary Semi-Barker codes and Matched filters

A shift register whose outputs are tied in a specific pattern to +Vcc via resistors so that the output is maximum when the pattern is fully present in it is called a matched filter or an auto-correlation filter. The output is lower than +Vcc at all other instants.

Complementary Semi-Barker codes respond to matched filters in such a way that when the codes are passed through the matched filters and then added, the voltage is maximum when the entire code is present in the filter. At all other instances, the voltage is less than half the maximum value. In an ideal situation, the voltage has to be zero symmetrically on either side of the maximum value. Due to this attribute of these codes, we utilize them to encrypt the signal.

Semi-Barker codes and their complements can be produced from their basic two-bit codes, 10 and 11. A four-bit code can be produced as follows:

Both the codes are written together as 1011 and 1110. Their complements are 1000 and 1101 respectively. That is, the first two bits are taken as they are and the last two bits are inverted. With these as the base, one can generate codes of length 8, 16, 32 and so on.

For this project, a pair of complementary codes of length 16 each, was chosen. They are: 1110 1101 1110 0010 and 1110 1101 0001 1101.

For convenience, consider a 4-bit code, 1101 and its complement 1110. The connections are shown for the code 1101[figure 2.6]. Similar connections are to be done for its complement.

			1	1	0	1				Voltage
1	1	0	1	x	x	x				1
	1	1	0	1	x	x				0
		1	1	0	1	x				-1
			1	1	0	1				4
			x	1	1	0	1			-1
			x	x	1	1	0	1		0
			x	x	x	1	1	0	1	1

Table a

			1	1	1	0				Voltage
1	1	1	0	x	x	x				-1
	1	1	1	0	x	x				0
		1	1	1	0	x				1
			1	1	1	0				4
			x	1	1	1	0			1
			x	x	1	1	1	0		0
			x	x	x	1	1	1	0	-1

*Table b**Table 2.3* Tables to show working of an auto-correlation filter

Tables 2.3a&b show the working of the matched filters. The codes can be seen shifting in and out of the filters [the second broad column represents the filter]. "x" represents the noise. For every instant that the data shifts in, each bit contributes a positive or negative high, depending on whether it matches the connection in the filter. The last column shows the sum at each instant.

It is to be noticed that the voltages are complementary to each other except at the instant when the entire code is present, in which case it is maximum. Hence when these voltages are added, the side-voltages are cancelled and the main voltage doubles. This concept is used to detect a pair of 16-bit Complementary Semi-Barker codes.

2.7 Clipping circuits

The configuration used in this project is called a biased diode clipper as it provides partial clipping of the input wave-forms. The diode in the following circuit is reverse biased by the Variable dc voltage source. The dc voltage source maintains the cathode at a positive potential with respect to its anode. The diode remains off until the input voltage is more positive than the sum [say $+V_1$] of the voltage at the variable dc and the forward voltage drop, which is 0.7 V. When the input voltage exceeds $+V_1$, the diode conducts and limits the output voltage to a maximum voltage value of V_1 . When the input voltage is less than $+V_1$, the diode acts as an open switch and the input voltage equals the output voltage. This kind of a circuit clips only a part of the positive peak, depending on the value of the variable dc voltage.

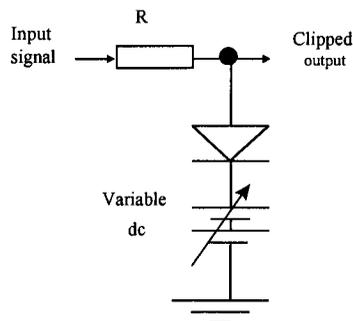


Figure 2.7 *Biased diode clipping circuit*

This circuit is used at the receiver. The detected signal has a distinctly large pulse at equal intervals of time. At this stage a threshold voltage is set to clip off the undesired signal. This clipped signal represents a traditional radar signal.

3.1 Introduction

The first step is to have a signal comprising of binary noise with the codes embedded in it in equal intervals of time. First the codes and the noise have to be generated. Then one needs a switch that alternates between them such that it stays on the codes for 32 clock pulses [since the length of both the codes together is 32] and on the binary noise for a long time. Since a mod-512 counter is used to control the switch, the switch should stay on the codes for 32 clock pulses and on the noise for the remaining 480 clock pulses.

On the above grounds, the transmitter has the following sections:

- A circuit to generate the noise
- A circuit to generate the codes and
- A switch controlled by signals to alternate the transmission of the two

The following sections discuss each part of the transmitter in detail .

3. TRANSMITTER

3.1 Introduction

The first step is to have a signal comprising of binary noise with the codes embedded in it in equal intervals of time. First the codes and the noise have to be generated. Then one needs a switch that alternates between them such that it stays on the codes for 32 clock pulses [since the length of both the codes together is 32] and on the binary noise for a long time. Since a mod-512 counter is used to control the switch, the switch should stay on the codes for 32 clock pulses and on the noise for the remaining 480 clock pulses.

On the above grounds, the transmitter has the following sections:

- A circuit to generate the noise

- A circuit to generate the codes and

- A switch controlled by signals to alternate the transmission of the two

The following sections discuss each part of the transmitter in detail.

3.2 Generation of noise

The first block to be considered in the transmitter is the maximum length sequence or noise. It is generated by a modulo-2 feedback shift register .

Modulo-2 addition is defined as follows:

$$0 \oplus 0 = 0$$

$$1 \oplus 0 = 1$$

$$0 \oplus 1 = 1$$

$$1 \oplus 1 = 0$$

Certain pre-determined sections of a shift register are combined for modulo-2 addition, the resultant is fed back as input to the first section and the process goes on. The number of feedback combinations is finite because each stage uniquely determines its following stage. With a proper feedback combination, a shift register with " k " sections, can have two possible sets of outputs depending on the input initially given . If the initial input consists of only zeros, the output will be a zero sequence of length 1. For any other initial input , we have as many as $2^k - 1$ outputs and this output is called a maximum length sequence.

In this project a 16 section-shift register is used. To obtain a maximum length sequence, it is necessary to determine the appropriate sections for feedback . This can be tedious for 16 sections when done manually. A program in Q-BASIC was developed to give the possible feedback combinations [Appendix C].

3.3 Generation of codes

During transmission of signals, there is always a danger that wanted signals could be masked out by undesired signals. Digital electronics has made it possible to produce encrypted signals that cannot be easily recognized as radar pulses by any intelligent target. Phase coding within a transmitted pulse is often used in radar and communication systems in order to spread the signal bandwidth. Some code sequences, when received in an appropriate compression filter, can give appreciable processing gain. But a major disadvantage of this method is that the compressed pulse invariably has side lobes, which limit the dynamic range of closely spaced targets.

The need to suppress the side-lobes and prevent masking of wanted signals is obvious. This is accomplished by hiding binary codes (known only to the sender) in the pseudo-random sequence transmitted by the radar. The hidden binary code is retrieved from the reflected signal by auto-correlation techniques.

There is a possibility that the pattern of the code appears in the maximum length sequence as well. This will give rise to "false alarms". To overcome this difficulty, a pair of complementary codes is used. Two 16-bit, complementary Semi-Barker codes are used.

Two 16-1 multiplexers are connected as one 32-1 multiplexer to generate the codes.

In this project a pair of complementary Semi-Barker codes is used because of the way they respond to auto-correlation filters, easing the process of detection at the receiver.

CODES

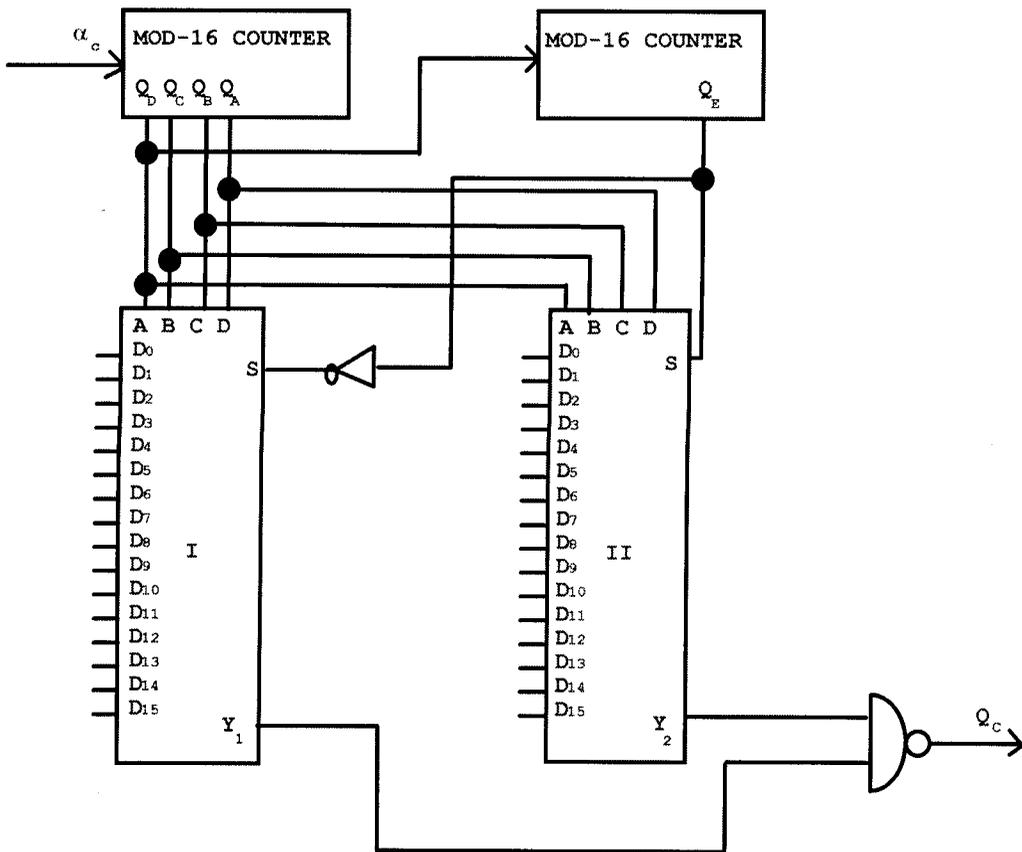


Figure 3.1 Generation of the codes

Two mod-16 counters are connected to act as a mod-32 counter. Q_A, Q_B, Q_C and Q_D are the control signals for the two multiplexers [I and II]. The multiplexers used are IC 74150. D_0 to D_{15} of " I " are the data bits of the first code and those of " II " are the data bits of its complementary code. " S " is the strobe input. The strobes of both the multiplexers are controlled in such a way that they remain active for 16 clock pulses only. When one is active [low], the other is not active [high] and vice-versa. For IC74150, Y is complementary to the data, therefore the output Q_C of the NAND gate will be the data itself.

3.4 Control signals

We have signals that control the way the codes and the binary noise are transmitted. A mod-512 counter acts as a clock to the Enable flip-flop. Hence the outputs should share these 512 counts in such a way that one output remains high for as long as the noise comes in and the other should be high long enough to send the codes. Since we use a pair of complementary codes, each of length 16 bits, the enable signal for the codes should be active for 32 clock pulses and that of the binary noise for the remaining 480 clock pulses.

Figure 3.2 shows the working of the control signals.

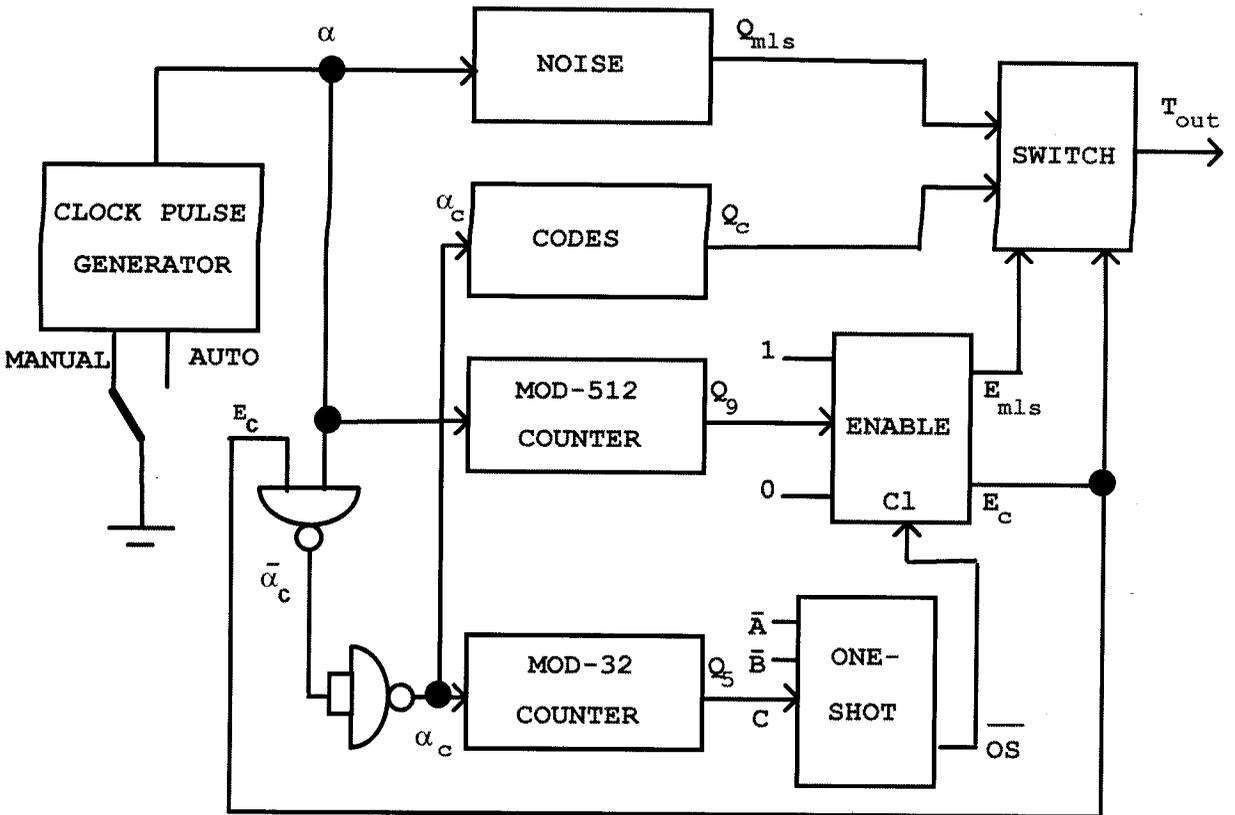


Figure 3.2 Transmitter control signals

The control signals can be classified into three parts: the counters, the enable flip-flop and the one-shot. There are two counters used, one is a mod-512 counter and the other is a mod-32 counter. The output of the mod-512 counter acts as a clock to the enable flip-flop. The outputs of the enable are called E_{mls} and E_c [Q and its complement respectively]. At the instant when E_c goes high, it activates the mod-32 counter, thereby the one-shot triggers and in turn sends a negative pulse to the clear input of the enable flip-flop after 32 clock pulses. This resets the flip-flop for the remaining time and the process repeats.

3.5 Switch

It can be seen that the enable signals for the codes and the binary noise go high and low for 32 and 480 clock pulses respectively and the process repeats. When E_{mls} goes high, we have the binary noise as T_{out} and when E_c goes high, the codes are transmitted as can be understood from figure 3.3.

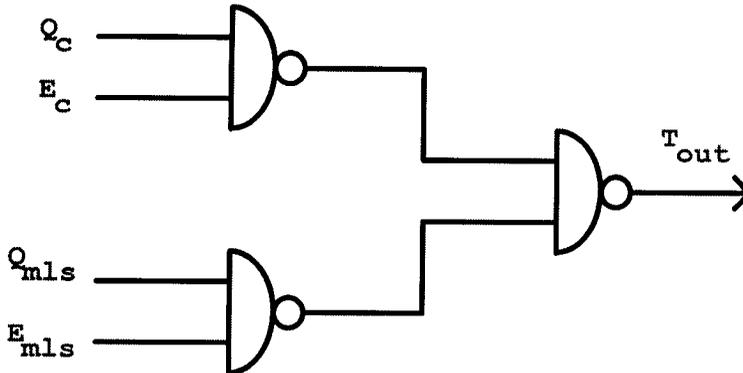


Figure 3.3 *Switch*

The entire transmitter is shown in figure 3.4.

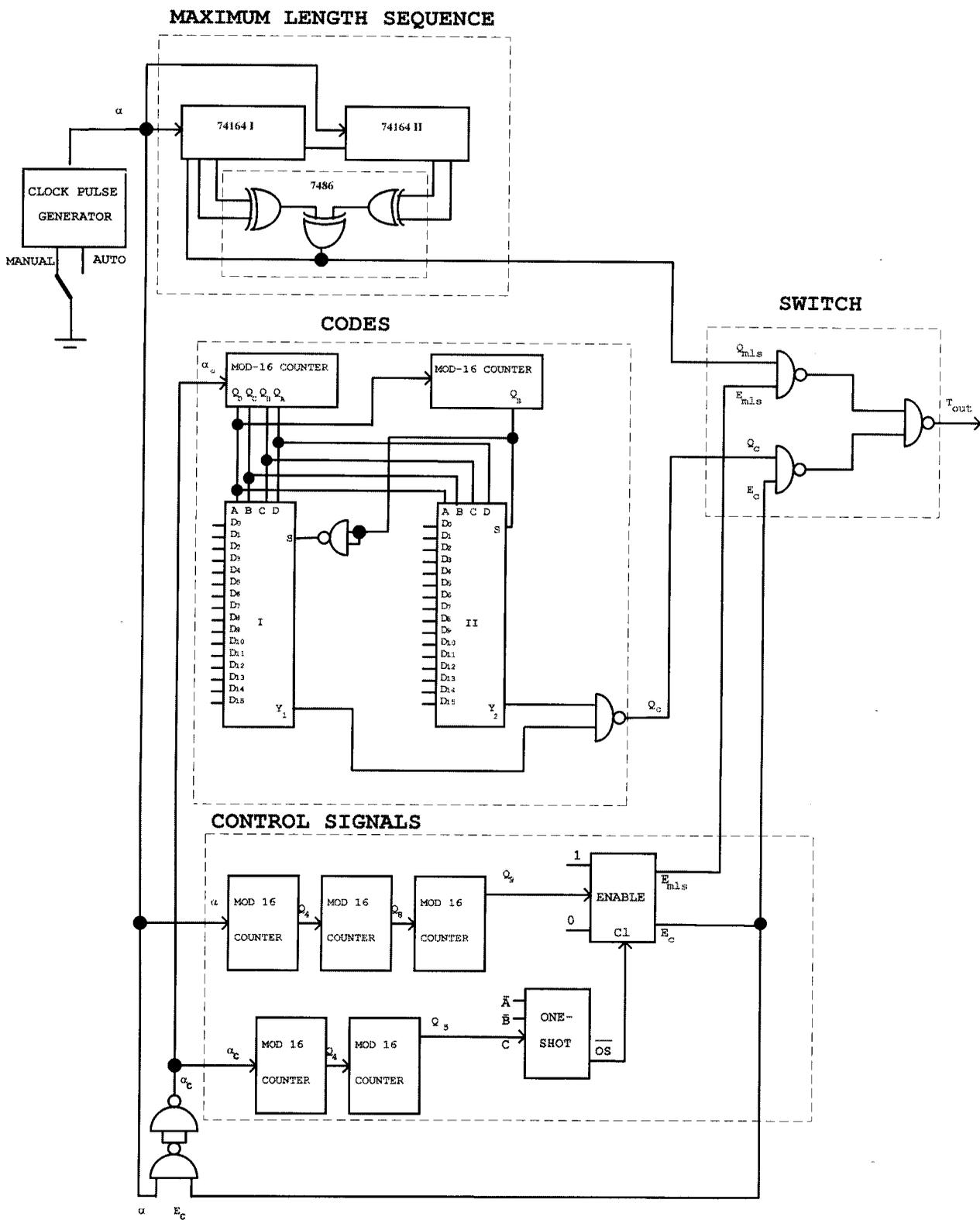


Figure 3.4 Detailed diagram of the entire transmitter

3.6 Discussion

The first intent of the project to generate a signal comprising of the binary noise and the codes was successfully accomplished.

One of the major problems encountered was due to the “fan-out”, i.e., the maximum number of TTL loads a TTL device can reliably drive. It is usually “10”. The clock, α , drives a number of devices. But this was handled. The clock was made to activate 10 inverters first, each of which was later input to various sections [figure 3.5].

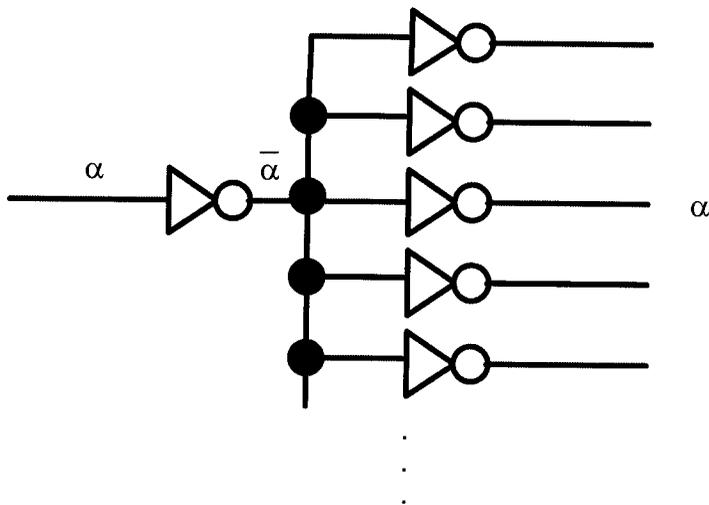


Figure 3.5 *Solution for fan-out*

4.1 Introduction

The receiver does the most important part, i.e., detecting the echo by a technique called auto-correlation. The idea is to pass the signal which contains binary noise and a pair of complementary Semi- Barker codes through a matched filter and then add them. Since what is required is a condition where both the codes are simultaneously present at an adder, two auto-correlation filters [with 16 sections each] are used to identify the two codes simultaneously. The resultant should have a distinct pulse every time the codes are completely present in their respective filters.

The next step is to set a threshold voltage level to cut off the undesired output and to obtain a signal that exactly resembles a traditional radar signal.

4. RECEIVER

4.1 Introduction

The receiver does the most important part, i.e., detecting the echo by a technique called auto-correlation. The idea is to pass the signal which contains binary noise and a pair of complementary Semi- Barker codes through a matched filter and then add them. Since what is required is a condition where both the codes are simultaneously present at an adder, two auto-correlation filters [with 16 sections each] are used to identify the two codes simultaneously. The resultant should have a distinct pulse every time the codes are completely present in their respective filters.

The next step is to set a threshold voltage level to cut off the undesired output and to obtain a signal that exactly resembles a traditional radar signal.

4.2 Auto-correlation filters

The main idea used to detect the echo is what is called auto-correlation technique using matched filters. A matched filter is a shift-register whose outputs, or their complements accordingly, are matched to a specific code. The filters are connected in a similar fashion as shown in figure 2.6.

The output of the filters is maximum when the codes are completely present in their respective shift registers. The two 16-bit shift registers required were realised using four IC 74164 chips.

IC 74164 is an eight bit Serial-In-Parallel-Out shift register.

4.3 Delay and Adders

As mentioned in the 'Abstract', a delay is required. Two IC-7491 chips are used for this purpose. IC 7491 is an eight bit shift register which causes a 16-bit delay [that is, long enough to delay the signal so that at a particular instant, both codes appear at the adder simultaneously]. It has two data inputs. Either of them can be used as an input and the other should be tied to +Vcc. The output of the delay circuit is input to the auto-correlation Filter1. The outputs from both the filters are added to complete the detection. IC741 which is an operational amplifier, is used for addition. Figure 4.1 shows the components and appropriate connections.

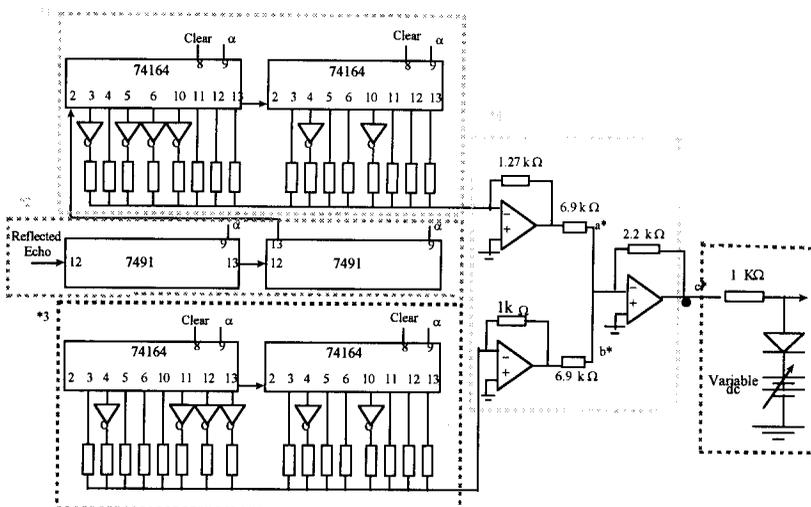


Figure 4.1 Detailed diagram of the receiver

The filters are “matched” to the codes to give maximum voltage at the output when the codes are present in them. This can be seen from the observations shown in Table 4.1. The outputs [of each filter] are then added to give twice the voltage. This voltage is maximum when the codes appear in their respective filters. Notice that feedback resistors used for adding the output of both the filters have different values. This can be explained as follows: Due to the tolerance of the resistors, the scale of both the added outputs are not of same magnitude. The aim is addition of voltages of equal values. In order to bring the outputs of both the filters to a consistent scale, the feedback resistors have different values. The outputs at a*, b* and c* [figure 4.1] are shown in figure 4.2.

Table 4.1 shows the observations made at the receiver:

No.	Output of Filter 1	Output of Filter 2	Sum
1	0.2	0.6	-0.8
2	0.2	1.6	-1.8
3	0.2	0.6	-0.8
4	0.8	-0.2	-0.6
5	0.2	-3.2	3
6	0.2	-0.2	0
7	2.4	-3.4	1
8	1.8	-0.6	-1.2
9	0.2	-0.4	0.2
10	1	-0.6	-0.4
11	0.2	1	-1.2
12	-0.2	-0.6	0.8
13	0.2	1.8	-2
14	0.2	-0.6	0.4
15	-1	0.4	0.6
16	0.2	-0.2	0
17	-0.2	0.2	0
18	-6	-6	12
19	-1.2	0.2	1
20	-1.2	-0.6	1.8
21	-1.2	0.2	1
22	0.2	0.2	-0.4
23	-1.2	1	0.2
24	-2.4	0.2	2.2
25	-1.2	0.2	1
26	-3.2	-0.6	3.8
27	-1.2	0.8	0.4
28	-0.2	-0.6	0.8
29	-1.2	-2.8	4
30	-3.2	0.2	3

Table 4.1 Voltage values as the codes shift in and out of their respective filters

The entire code is matched exactly 32 clock pulses after the first bit gets shifted in the filter. Table 4.1 shows a part of the shifting in and a part of the shifting out of the codes and the corresponding voltages at the outputs of both the filters at each instant. The values in the second and third columns are inverted because the op-amp is used in its inverting configuration for addition. Similarly, in the fourth column, the values are positive because here, negative voltages are added using an op-amp in its inverting mode, and the result is positive. The outputs from both the filters are further added to get a distinct pulse[or the main lobe]. It can be seen that the length of the longest side-lobe, is 4V, which is very small when compared to the length of the main-lobe [12V].

Figure 4.2 is a graph of the values shown in table 4.1.

4.4 Setting a threshold level

Output of Filter 1

The next step is to set a threshold level for the detected echo. This is done by introducing a clip

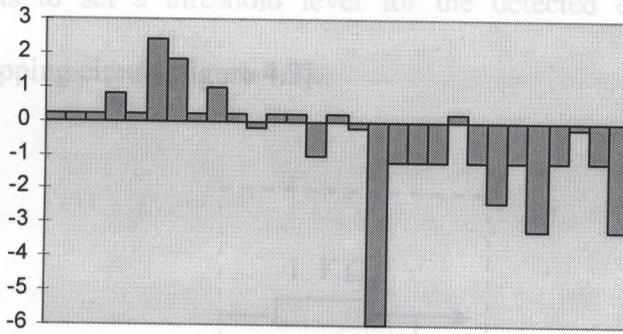


Figure {a*}

Output of Filter 2

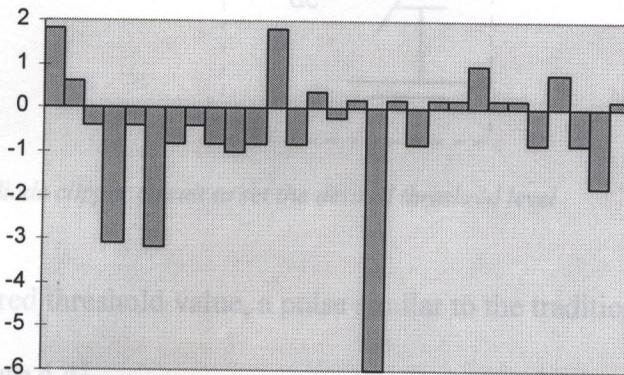


Figure {b*}

Addition of the voltages at the output of both the filters

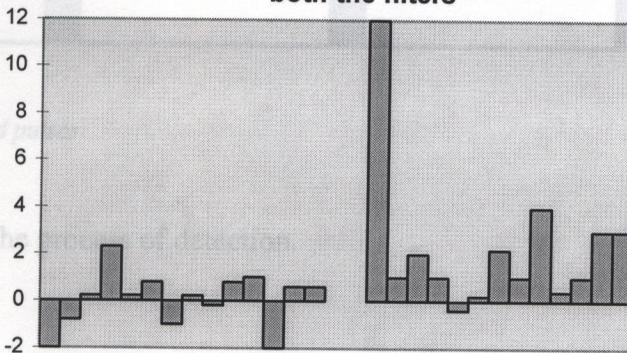


Figure {c*}

Figure 4.2 Outputs at the receiver

4.4 Setting a threshold level

The next step is to set a threshold level for the detected echo. This is done by introducing a clipping circuit [figure 4.3].

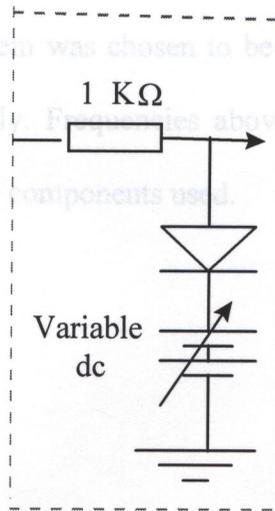


Figure 4.3 Biased diode clipper circuit to set the desired threshold level

By setting a desired threshold value, a pulse similar to the traditional radar pulse could be retrieved [figure 4.4].



Figure 4.4 Detected pulses

This completes the process of detection.

4.5 Discussion

The chief objective of the receiver was to identify the codes and indicate their presence. Two matched filters successfully identified the codes and indicated their presence by a distinct pulse.

The clock frequency of the system was chosen to be 20kHz. The effect of the process described are shown very clearly. Frequencies above 40kHz show a deterioration in performance due to the hardware components used.

5.1 Introduction

Reception of a signal in a telecommunication system may be marred by noise, which can originate from a variety of sources. It is necessary for any system to remain as much unaffected by disturbances as possible.

In this project, a channel is introduced to add disturbances to the output of the transmitter. This represents the natural disturbances that may affect the signal. The effect of this disturbance can be noticed at the receiver by the changes in the magnitude of the main lobe. The robustness of the system can be determined by the amount of this disturbance it would take to vanish the main lobe completely. A signal generator's square wave output is used to produce the disturbance.

5. CHANNEL

5.1 Introduction

Reception of a signal in a telecommunication system may be marred by noise, which can originate from a variety of sources. It is necessary for any system to remain as much unaffected by disturbances as possible.

In this project, a channel is introduced to add disturbances to the output of the transmitter. This represents the natural disturbances that may affect the signal. The effect of this disturbance can be noticed at the receiver by the changes in the magnitude of the main lobe. The robustness of the system can be determined by the amount of this disturbance it would take to vanish the main lobe completely. A signal generator's square wave output is used to produce the disturbance.

5.2 Addition of disturbance to the output of the transmitter

The purpose of the channel is to introduce some pulses by adding them to the transmitted signal $[T_{out}]$. A signal whose frequency can be varied is fed as an input to a one-shot. The output of the one-shot is mixed with T_{out} [figure 5.1]. The width of this pulse is made almost equal to the pulse-width of T_{out} .

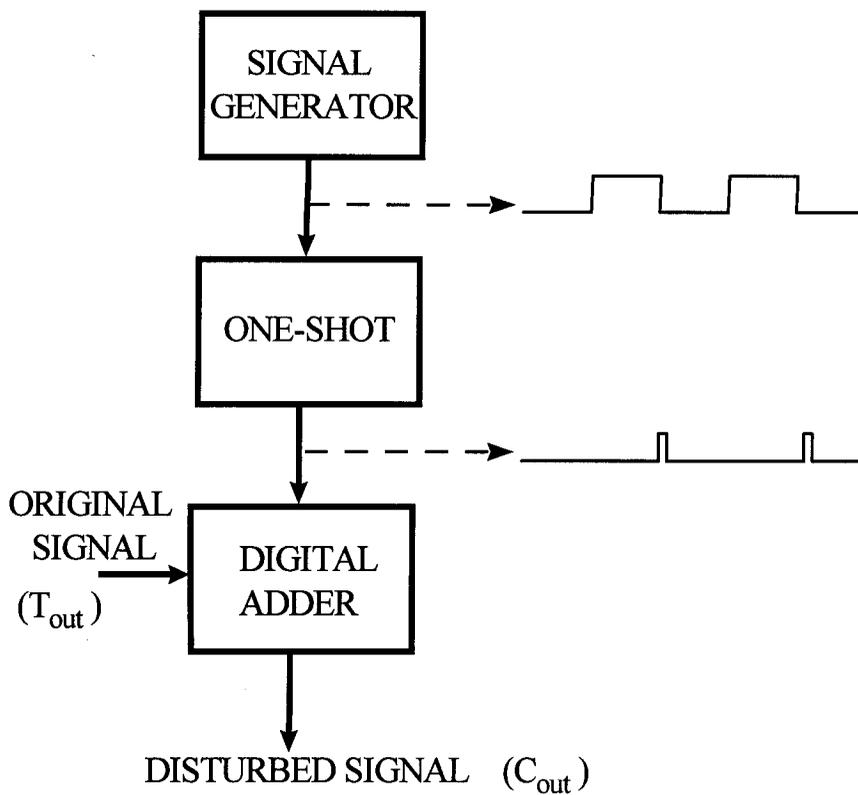


Figure 5.1 Introduction of disturbance in the original signal

5.3 Discussion

The disturbance pulses are to be introduced into the system through a NAND gate [figure 5.2].

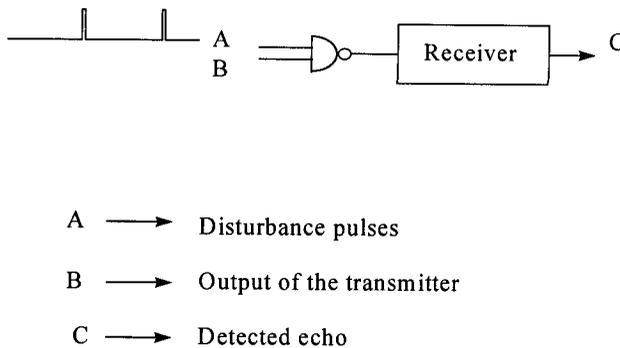


Figure 5.2 Addition of pulses via a NAND gate

The number of pulses introduced depends on the frequency of the disturbance signal. The higher the frequency, the more the number of pulses introduced. When the amount of disturbance is increased, the length of the main-lobe begins to decrease. It can be seen [table 5.1] that for very high frequencies of the disturbance signal, the length of the main lobe becomes so small that it disappears among the side-lobes. This was observed when the frequency of the disturbance signal exceeded 3kHz.

There were three main objectives in the project:

1. to construct a signal comprising of binary noise and a pair of suitable codes in a definite pattern,
2. to have a circuit detect the codes in the signal and indicate their presence with a pulse and,
3. to check the sensitivity and robustness of the system by introducing a channel of external disturbance.

A modulo-2 feedback shift register generated a pseudo-random sequence of binary digits [noise]. Using two shift registers the desired codes set as their data inputs the codes were generated. The noise and the codes were then mixed in the desired pattern. This was done effectively.

By using auto-correlation technique, the signal comprising of noise and codes was detected. This detected pulse was clipped off at a certain voltage level to resemble the traditional radar pulse. This was accomplished efficiently. At this stage, a real radar system can identify the target as done in the conventional way.

Disturbance was introduced to inspect the endurance of the detected pulse. This was sturdy for frequencies of the disturbance signal less than 3kHz. Beyond this, the length of the main-lobe became almost equal to the length of the noise generated by the disturbance signal, thus making it disappear in the noise.

6. CONCLUSION

There were three main objectives in the project:

1. to construct a signal comprising of binary noise and a pair of suitable codes in a definite pattern,
2. to have a circuit detect the codes in the signal and indicate their presence with a pulse and,
3. to check the sensitivity and robustness of the system by introducing a channel of external disturbance.

A modulo-2 feedback shift register generated a pseudo-random sequence of binary digits [noise]. Using multiplexers with the desired codes set as their data inputs the codes were generated. The noise and the codes were then mixed in the desired pattern. This was done effectively.

By using auto-correlation technique, the signal comprising of noise and codes was detected. This detected pulse was clipped off at a certain voltage level to resemble the traditional radar pulse. This was accomplished efficiently. At this stage, a real radar system can identify the target as done in the conventional way.

Disturbance was introduced to inspect the endurance of the detected pulse. This was sturdy for frequencies of the disturbance signal less than 3kHz. Beyond this, the length of the main-lobe became almost equal to the length of the noise generated by the disturbance signal, thus making it disappear in the noise.

- [1] Ackroyd M.H. and Ghani F., *IEEE, Volume AES-9, No.2, 1973*
Optimum mismatched filters for side lobe suppression
- [2] Beckman D., *Royal Military Academy, The Netherlands, 1969*
Maximum length sequences
- [3] Cloke J.A., *Royal Air Force, Ministry Of Defence, UK, IEEE, 1982*
Ambiguity functions of Complementary Series
- [4] Frederick L. Gould, *McGraw Hill Inc., 1995*
Radar for technicians
- [5] Jacob Millman, *McGraw Hill Inc., 1971*
Integrated Electronics
- [6] Malvino A.P. and Leach D., *McGraw Hill Inc., 1991*
Digital principles and applications
- [7] Merrill I. Sidolaft, *McGraw Hill Inc., 1962*
Introduction to radar systems
- [8] Mora J.L. et al, *The University of El Paso, SPIE, Volume 2275*
Sub-optimum binary phase code search using a genetic algorithm
- [9] Ridenour L.N., *Academic Press Inc., 1967*
Radar Signals
- [10] Rihaczek A.W. and Golden R.M., *IEEE, Volume AES7-9, No.6, 1971*
Range Side Lobe suppression for Barker codes

7. REFERENCES

- [1] **Ackroyd M.H. and Ghani F.**, *IEEE, Volume AES-9, No.2, 1973*
Optimum mismatched filters for side lobe suppression
- [2] **Beekman D.**, *Royal Military Academy, The Netherlands, 1969*
Maximum length sequences
- [3] **Cloke J.A.**, *Royal Air Force, Ministry Of Defence, UK, IEEE, 1982*
Ambiguity functions of Complementary Series
- [4] **Frederick L. Gould**, *McGraw Hill Inc., 1995*
Radar for technicians
- [5] **Jacob Millman**, *McGraw Hill Inc., 1971*
Integrated Electronics
- [6] **Malvino A.P. and Leach D.**, *McGraw Hill Inc., 1991*
Digital principles and applications
- [7] **Merril I. Silolnik**, *McGraw Hill Inc., 1962*
Introduction to radar systems
- [8] **Mora J.L. et al**, *The University of El Paso, SPIE, Volume 2275*
Sub-optimum binary phase code search using a genetic algorithm
- [9] **Ridenour L.N.**, *Academic Press Inc., 1967*
Radar Signals
- [10] **Rihaczek A.W. and Golden R.M.**, *IEEE, Volume AES7-9, No.6, 1971*
Range Side Lobe suppression for Barker codes

Auto-correlation filter. A shift register whose outputs are tied in a specific pattern to $+V_{cc}$ via resistors so that the output is maximum when the pattern is fully present in it is called a matched filter or an auto-correlation filter. The output is lesser than $+V_{cc}$ at all other instants.

Binary numbers. A number code that uses only the digits 0 and 1 to represent quantities.

Clipping circuit, a circuit that clips off a part of the input voltage.

Clock, A periodic wave (usually a square wave) that is used to as a synchronizing signal in a digital system.

Complementary Symmetric codes. Codes which, when passed through matched filters and added ~~equivalently~~ produce cancelled side-lobes and a doubled main lobe at the instant they are ~~completely~~ present in the filters.

Counter, A counter is a circuit which, when driven by a clock can be used to count the number of clock cycles.

Detection, in this case, it means retrieving the pulse.

Fan-out, The maximum number of TTL loads a TTL device can reliably drive.

Flip-flop, An electronic circuit that has two stable states.

Matched filter, see *Auto correlation filter*.

Maximum length sequence. When certain sections of a shift register are combined for mod-2 addition and the resultant is fed back to the first section we get a random sequence. When the length of such a sequence generated by a k-section-wide shift register is $2^k - 1$, it is called a maximum length sequence.

Modulus, It is the total number of states that a counter can progress.

8. GLOSSARY

Auto-correlation filter, A shift register whose outputs are tied in a specific pattern to +Vcc via resistors so that the output is maximum when the pattern is fully present in it is called a matched filter or an auto-correlation filter. The output is lesser than +Vcc at all other instants.

Binary numbers, A number code that uses only the digits 0 and 1 to represent quantities.

Clipping circuit, a circuit that clips off a part of the input voltage.

Clock, A periodic wave-form (usually a square wave) that is used to as a synchronizing signal in a digital system.

Complementary Semi-Barker codes, Codes which, when passed through matched filters and added simultaneously, produce cancelled side-lobes and a doubled main lobe at the instant they are completely present in the filters.

Counter, A counter is a circuit which, when driven by a clock can be used to count the number of clock cycles.

Detection, In this case, it means retrieving the pulse.

Fan-out, The maximum number of TTL loads a TTL device can reliably drive.

Flip-flop, An electronic circuit that has two stable states.

Matched filter, see *Auto correlation filter*.

Maximum length sequence, When certain sections of a shift register are combined for mod-2 addition and the resultant is fed back to the first section we get a random sequence. When the length of such a sequence generated by a k-section-wide shift register is $2^k - 1$, it is called a maximum length sequence.

Modulus, It is the total number of states that a counter can progress.

Multiplexer, It is a circuit that selects one data bit from several inputs, controlled by certain signals.

One-shot, Circuits which have one stable state and one quasi-stable state are called switching circuits or one-shots.

Operational amplifier, An operational amplifier is a circuit which is chiefly used for mathematical operations.

Pseudo-random sequence, When certain sections of a shift register are combined for mod-2 addition and the resultant is fed back to the first section we get a pseudo-random sequence. Since each resultant is uniquely determined by its previous stage, the sequence repeats itself and hence the name.

Shift register, A group of flip-flops connected in such a way that a binary number can be shifted into or out of the flip-flops.

Switching circuit, Circuits that change states periodically.

Zero-sequence, In a modulo-2 feedback shift register, if the initial condition in the shift register is all zeros, then the sequence so generated has nothing but zeros. Such a sequence is called a zero-sequence.

A. List of ICs, test equipment and other components used

IC741, an operational amplifier

IC7400, a quad 2-input NAND gate

IC7473, a dual JK flip-flop with clear

IC7486, a dual, 2-input Ex-OR gate

IC7491, an 8-bit serial-in-serial-out shift register

IC7493, a 4-bit binary counter

IC74121, a one-shot

IC74150, a 16 to 1 multiplexer

IC74164, an 8-bit parallel load shift register with clear

Resistors [10k Ω , 6.8k Ω , 6.2k Ω , 2.2k Ω , 1k Ω]

Capacitors [1 μ f, 10nf]

Debug boards

Power supply unit [TEKNIKIT CONSOLETTTE, TK286]

Oscilloscope [PHILIPS, PM3208]

SINE SQUARE OSCILLATOR [SSO 603]

FUNCTION GENERATOR [FG 600]

9. APPENDICES

A. List of ICs, test equipment and other components used

IC741, an operational amplifier

IC7400, a quad 2-input NAND gate

IC7473, a dual JK flip-flop with clear

IC7486, a dual, 2-input Ex-OR gate

IC7491, an 8-bit serial-in-serial-out shift register

IC7493, a 4-bit binary counter

IC74121, a one-shot

IC74150, a 16 to 1 multiplexer

IC74164, an 8-bit parallel load shift register with clear

Resistors [10k Ω , 6.8k Ω , 6.2k Ω , 2.2k Ω , 1k Ω]

Capacitors [1 μ f, 10nf]

Debug boards

Power supply unit [TEKNIKIT CONSOLETTTE, TK286]

Oscilloscope [PHILIPS, PM3208]

SINE SQUARE OSCILLATOR [SSO 603]

FUNCTION GENERATOR [FG 600]

B. Example to show the working of a modulo-2 feedback shift register

Let us consider a shift register with four sections with the initial condition 0001, i.e., the shift register has “0001” stored in it at the time we consider it.

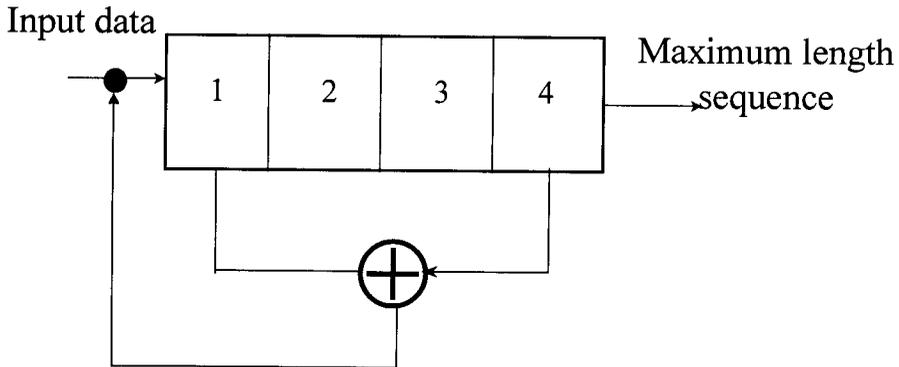


Figure. 9.1 Modulo-2 feedback addition of a 4-section shift register

The initial condition is 0001

So, when the data in the first and last sections are added [modulo-2 addition], the resultant is $0 \oplus 1 = 1$

This is input to the first section and all the other bits shift one place to the right.

Hence, the condition is now 1000. This process continues and we can see that after 15 stages, the initial condition is repeated. Notice that this combination of modulo-2 feedback gives a maximum length sequence, i.e., a sequence of length $[2^4 - 1]$, 15.

We can see the way the data changes in the shift register for this particular feedback combination:

1.	0	0	0	1	$0 \oplus 1 = 1$
2.	1	0	0	0	$1 \oplus 0 = 1$
3.	1	1	0	0	$1 \oplus 0 = 1$
4.	1	1	1	0	$1 \oplus 0 = 1$
5.	1	1	1	1	$1 \oplus 1 = 0$
6.	0	1	1	1	$0 \oplus 1 = 1$
7.	1	0	1	1	$1 \oplus 1 = 0$
8.	0	1	0	1	$0 \oplus 1 = 1$
9.	1	0	1	0	$1 \oplus 0 = 1$
10.	1	1	0	1	$1 \oplus 1 = 0$
11.	0	1	1	0	$0 \oplus 0 = 0$
12.	0	0	1	1	$0 \oplus 1 = 1$
13.	1	0	0	1	$1 \oplus 1 = 0$
14.	0	1	0	0	$0 \oplus 0 = 0$
15.	0	0	1	0	$0 \oplus 0 = 0$
	0	0	0	1	$0 \oplus 1 = 1$

C. A program in Q-BASIC to determine the feedback sections in a 16 bit shift register

```
REM DIMENSION STATEMENTS TO USE ARRAYS
```

```
    DIM A (1 TO 16)
```

```
    DIM T (1 TO 16)
```

```
    CLS
```

```
REM READING INITIAL CONDITION
```

```
    FOR I = 1 TO 15
```

```
        A(I) = 0
```

```
    NEXT I
```

```
    A(16) = 1
```

```
    CTR = 0
```

```
REM DEFINING ADDITION BY MODULO 2
```

```
    FOR I = 1 TO 13
```

```
        FOR J = I + 1 TO 14
```

```
            FOR K = J + 1 TO 15
```

```
10         T(I) = (A(16) + A(J) + A(K)) MOD 2
```

```
REM SHIFTING THE O/P BITS ONE PLACE TO THE RIGHT
```

```
    FOR J1 = 1 TO 12
```

```
        T(J1 + 1) = A(J1)
```

```
    FOR K1 = 1 TO 16
```

```
        A(K1) = T(K1)
```

```
    NEXT K1
```

```
    CTR = CTR + 1
```

```
REM CHECKING IF THE O/P HAS REACHED THE INITIAL CONDITION
```

```
FOR I1 = 1 TO 15
  IF A(I1) = 1 GO TO 10
NEXT I1

REM CHECKING IF THE SERIES IS A MAXIMUM LENGTH SEQUENCE
50  IF CTR = 65535 GO TO 70
60  CTR = 0
    NEXT K
    NEXT J
    NEXT I

REM PRINTING THE REQUIRED COMBINATION
70  PRINT "COUNTER ' CTR, I, J, K
    IF I > 13 GO TO 80
    GO TO 60

80  END
```